THREE-PHASE BOOST ACTIVE POWER FACTOR CORRECTION FOR DIODE RECTIFIERS

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This report documents an investigation and implementation of a 3 kW active power factor correction (pfc) design used to enable a diode rectifier to draw sinusoidal line currents with nearly unity power factor from a three-phase utility grid. The design utilizes a boost converter operating in discontinuous conduction mode to perform the pfc and dc regulation. The converter operates at a single frequency using pulse width modulation for dc voltage regulation. This active pfc design is compared to an equivalent conventional diode bridge rectifier supplying identical load without power factor correction to demonstrate the pfc function and benefits while highlighting issues that must be addressed when implementing pfc designs. The comparison of the two topologies is accomplished with resistive and constant power loading. The practical issues which render the proposed topology unfeasible for current commercial utilization are identified.

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FOREWORD

This report documents an investigation and implementation of a 3 kW active power factor correction (pfc) design used to enable a diode rectifier to draw sinusoidal line currents with nearly unity power factor from a three-phase utility grid. The design utilizes a boost converter operating in discontinuous conduction mode to perform the pfc and dc regulation.

This effort was accomplished by the Electrical Technology Section, Power Components Branch (POOC), Aerospace Power Division (POO), Aero Propolsion and Power Directorate, Wright Laboratory, Wright-Patterson Air Force Base, Ohio, under work unit 31452939, "Advanced Aircraft Electrical Power Generation and Distribution" with John G. Nairus leading the technical effort.

CHAPTER 1
INTRODUCTION

Power converters are used in power supplies, power conditioners, and motor drives. As a consequence they are currently in very wide use and recent improvements in power electronic devices, topologies, and controls are extending their range of application. In many of these applications, ac utility power is converted to dc by means of uncontrolled diode rectifiers that are driven by the ac line frequency. These rectifiers can be made controllable by replacing diodes with Silicon Controlled Rectifiers (SCR) to provide a controlled dc output when required. Though simple in design and high in efficiency, these conventional rectifiers produce problems in that they do not draw sinusoidal current from the utility source and inject current harmonics into the supply. This results in poor power factor seen by the utility and loads drawing poor power factor can disrupt other equipment connected to the same source. This is why utility companies today have power factor requirements. Power factor determines how much real power is drawn from the utility line. Power factor is defined as the ratio of average power to apparent power. Mohan in [1] defines power factor as

$$\mathrm{pf} = \left(\frac{I_{s1}}{I_s}\right)\mathrm{DPF}, \qquad (1)$$

$$\mathrm{DPF} = \cos\Phi_1 \qquad (2)$$

where I_{s1} is the rms value of the fundamental frequency component of the supply current, I_s is the rms value of the line current, DPF is known as the displacement power factor, and Φ_1 is the angle by which I_{s1} is displaced with respect to the input voltage. Thus it can be seen that power factor is affected by both harmonic distortion and displacement. In the

ideal case, the power factor is unity which means that only real power is supplied by the utility to a load that is, or appears as, resistive. Power factors less than unity indicate that reactive power is present with the real power. When reactive power is flowing in a circuit, it is not usable but still results in circuit power losses. Users are charged by utility companies for reactive power and equipment must be designed to handle it based on the power factor rating. Equipment that has poor power factor will be oversized (higher fabrication cost) and be expensive to operate. To illustrate this with an example, consider a 20 A, 120 Vac circuit. The maximum power that can be drawn from this circuit is 2400 W provided the power factor is unity. Decreasing the power factor will decrease the maximum power that can be drawn from that circuit without tripping circuit protection. If one had a load operating at 0.8 pf, then the maximum power that could be drawn without tripping circuit protection would be 1920 W. For this reason alone it is advantageous to draw high power factor. Utility requirements however also have cost penalties for not complying with power factor requirements and more requirements are being considered to specifically address excessive harmonic pollution of the utility supply.

When designing power factor correction (pfc) circuits, it is essential to recognize that both harmonic distortion and displacement contribute to power factor. If both of these are not considered in pfc design, a pfc circuit may lower the power factor. For example, most active pfc designs create switching harmonics when forcing the input current to be sinusoidal. If these harmonics are not properly managed, the result can be a low power factor even though the DPF is near unity. On the other hand, poor filter design could cause increased displacement thus lowering the DPF.

Recently active power factor correction techniques have become a popular topic both in academia and industry. Numerous publications have analyzed both single and three-phase topologies. Many papers have been published on different techniques and industry is being forced to produce equipment with high power factors and low harmonic distortion that does not pollute utility grids. Three-phase active pfc is used in higher power

applications and is the subject of this report. A popular classic active pfc design (both single and three-phase) is one that employs a boost converter operating in discontinuous conduction mode to perform the input current waveshaping and dc output voltage regulation. A three-phase version of this design is illustrated in Fig. 1. The boost converter

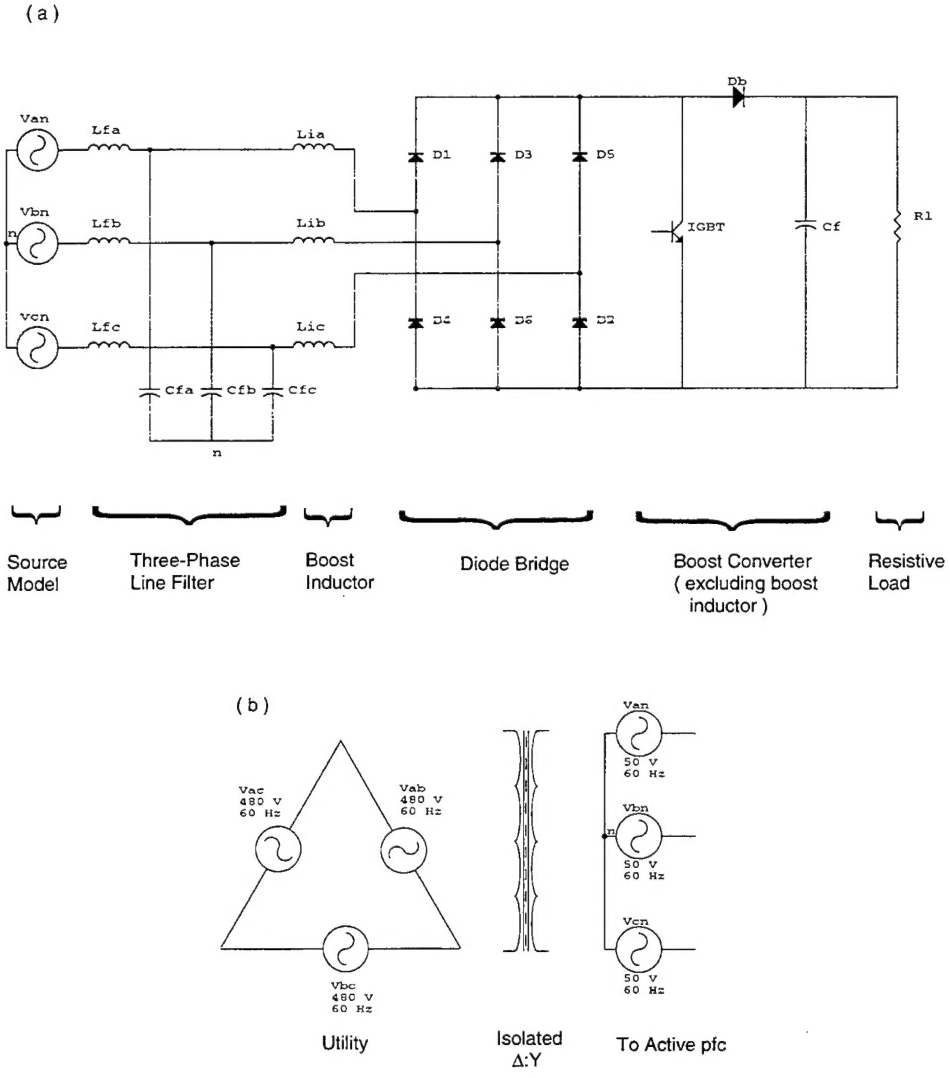


Fig. 1. (a) Active three-phase power factor correction circuit.
(b) Actual source implemented experimentally.

is built around the diode bridge and a three-phase input filter is added at the source output to filter switching harmonics generated by the boost circuit. The active waveshaping of the input current is performed when the Insulated Gate Bipolar Transistor (IGBT) boost switch

closes, shorting the source through the boost inductors, causing the source current to rise to a value proportional to the amplitude of the source voltage at the instant the switch closes. When the switch opens, the current in the boost inductor falls to zero. The boost converter operates at a frequency much greater than that of the source so that the switching harmonics created by it are easily filtered. The boost inductor is located at the input to the diode bridge otherwise the active pfc circuit will shape the current to the shape of the rectified voltage and would not force the input current to be sinusoidal. In addition to the active waveshaping, the boost converter is able to provide a regulated dc output.

Much of the work published on this active pfc approach has been developed on designs limited to approximately 1 kW of output power which does not require a three-phase source. The work has not shown the benefits and deficiencies that the more complex and expensive active pfc approaches possess over simpler, less expensive, and more efficient conventional rectifier designs. The problem with the work is that even though interesting concepts have been demonstrated, they have not been demonstrated with parameters that are practical outside of academia. The objective of this investigation was to design, simulate, build, and test a 3 kW boost pfc design and compare its performance to that of a simple unregulated rectifier to assess the feasibility of the proposed topology for commercial application. Both the active pfc circuit and the unregulated rectifier will be interfaced with utility power and a comparative assessment of their performance is presented here.

CHAPTER 2
ANALYSIS AND MODELING

This chapter presents the analysis and modeling of the three-phase boost active pfc rectifier design and the three-phase full-wave bridge rectifier design. The analysis relies on simulation and results in designs containing component values for experimental implementation of the two circuits.

2.1. THREE-PHASE BOOST ACTIVE POWER FACTOR CORRECTION RECTIFIER DESIGN

The pfc design described here utilizes a combination of analysis and simulation. The design process is based on the work of Prasad [2]. The converter will operate from a three-phase, 60 Hz, 480 Vac utility outlet. The designed output will be 270 Vdc rated for 3 kW. 270 Vdc was chosen because of its use by the military in aircraft and ground vehicles. In order to use the three-phase boost active pfc design shown in Fig. 1a, the source model voltage must be a value that will allow a boost of the rectified voltage to 270 Vdc at the load. A delta-wye isolation transformer was chosen that steps the 480 Vac down to 50 Vac to interface the active pfc circuit with the utility supply. This transformer ratio was selected because of its availability and the interface is shown in Fig. 1b. The three-phase 50 Vac results in 117 Vdc when rectified by a full-bridge diode rectifier which is a feasible value to boost-convert to 270 Vdc. An isolation transformer is also used because it is common practice for power supply vendors to incorporate them into their

designs. The computer modeling tool used in this investigation is Saber^{TM} [3] and ideal circuit components will be assumed for the design analysis.

The active pfc circuit is designed in sections. Some assumptions are made that influence the active pfc design. Referring to Fig. 1, the boost portion (boost inductors $L_{ia\text{-}c}$ and output capacitor C_{dc}) is designed followed by the three-phase LC input filter ($L_{fa\text{-}c}$ and $C_{fa\text{-}c}$). After all circuit values have been determined, the total pfc design will be simulated to verify the design.

2.1.1. DESIGN ASSUMPTIONS

The following assumptions for the converter are required to facilitate the design:

ac source rms per-phase voltage ($V_{an\ (rms)}$) = 50 V

supply frequency = 60 Hz

rated output power = 3 kW

From these assumptions, the per-phase rms source current is calculated:

$$I_{s_{rms}} = \frac{3000}{3 * 50} = 20A, \tag{3}$$

assuming 100 % efficiency.

2.1.2. BOOST INDUCTOR DESIGN

For analysis of the boost inductors $L_{ia\text{-}c}$, the input filter components are neglected. This is done because the boost converter needs to be designed first that will meet the output design specifications. Once the boost converter is in place, the input filter is designed to filter the switching harmonics generated by the converter. Since the design is a balanced three-phase topology, single-phase analysis will determine L_{ia} which will also equal L_{ib} and L_{ic} in Fig. 1. However the Saber^{TM} [3] model will be of the three-phase model shown

in Fig. 1a. Source current through the boost inductor can be determined by considering the circuit when the boost switch is on. When this occurs, the ac source (V_{an}) is essentially shorted through the boost inductor L_{ia}. Current through an inductor cannot change instantly and is defined by V = L(di/dt) which is the definition of inductance. When determining the boost inductance, the moment at which the input voltage is at its peak value is used because this will determine the maximum change of current through the inductor for a given length of time. Thus

$$V_{an(peak)} = L_{ia}\frac{di_{Lia(peak)}}{dt} \approx L_{ia}\frac{\Delta i_{Lia(peak)}}{\Delta t} \Rightarrow V_{an(peak)} = L_{ia}\frac{I_{ia(peak)}}{\Delta t} \qquad (4)$$

and Δt is the maximum time that the boost switch is on. The maximum switch on-time is chosen to correspond to a 50% switch duty cycle to provide sufficient time for the inductor current to fall to zero when the boost switch opens. The boost inductor current falls to zero during each switch cycle to keep the boost converter operating in a discontinuous conduction mode. This is illustrated in Fig. 2. Thus $\Delta t = T_b / 2 = 1/(2f_b)$ where f_b is the boost

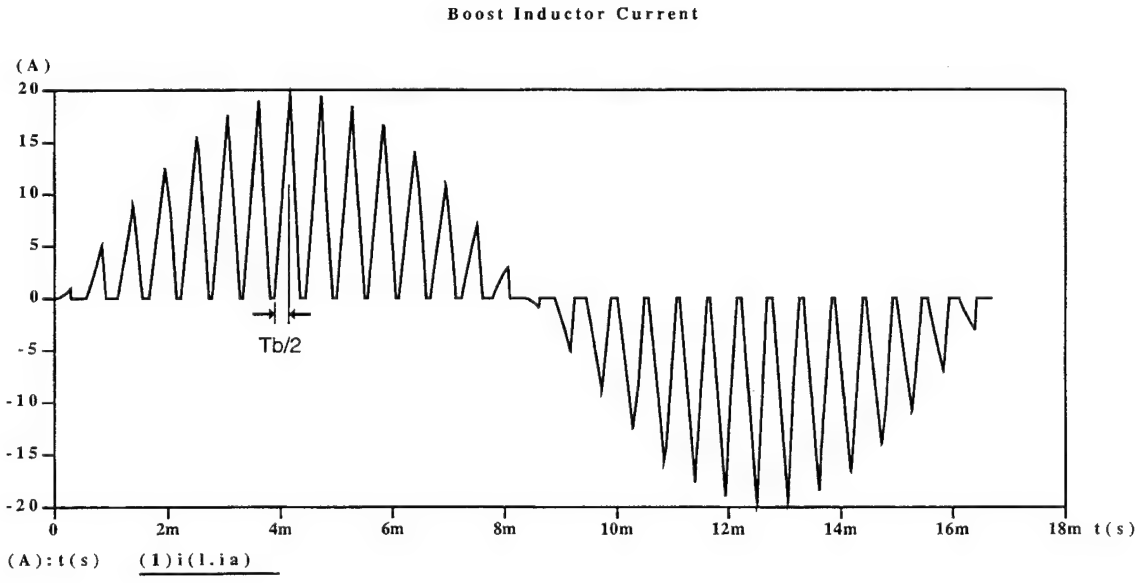


Fig. 2. Boost inductor current in the time domain.

switch frequency and T_b is the period of a boost cycle. Rearranging Eq. (4), the peak input current is defined as

$$I_{ia(peak)} = \frac{V_{an(peak)}}{L_{ia}} * \frac{T_b}{2}. \qquad (5)$$

Equation (5) is used to solve for the boost inductor value L_{ia} by finding a correlation between the rms source current in Eq. (3) and the peak input current ($I_{ia(peak)}$) in Eq. (5). This correlation is established by simulation. A simulation of the three-phase pfc circuit illustrated in Fig. 1 with the input filter components eliminated and a value of 100 μF arbitrarily chosen for the output capacitor is used. A boost frequency of 1800 Hz was used to generate Figs. 2 and 3 for illustration purposes. The node equations for this simulation are located in Appendix A. A value of boost inductance $L_{ia\text{-}c}$ was chosen in this simulation that resulted in per-phase peak source current equal to 20 A which is the value of rms source current.

The simulation transient response results in the time domain and frequency domain are found in Figs. 2 and 3 respectively. An analysis of these results yields the following estimates; the peak source current was 19.6 A and the magnitude of the 60 Hz fundamental component of the input current was 8.59 A. The ratio of the fundamental to peak

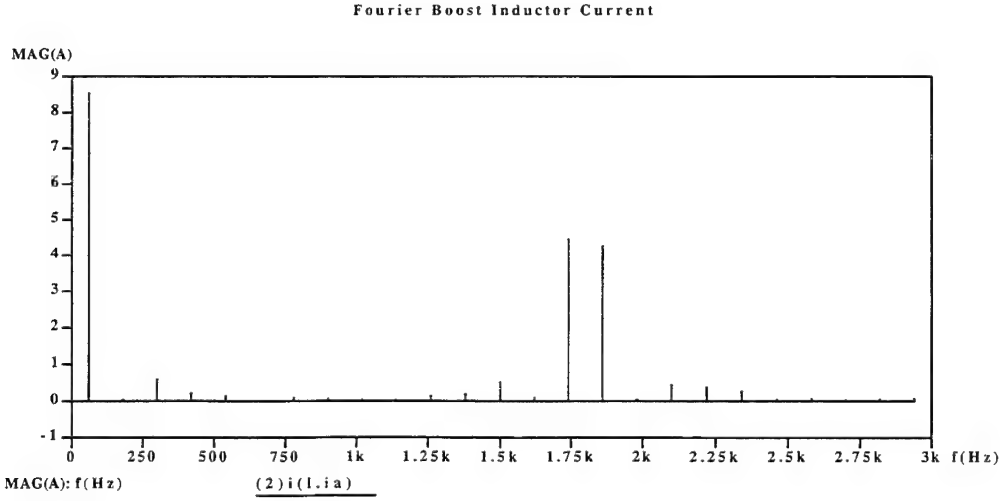


Fig. 3. Boost inductor current in the frequency domain.

magnitudes of the input current is 0.438. Thus

$$I_{srms} = 0.438 * I_{ia(peak)} \tag{6}$$

and L_{ia} is expressed as,

$$L_{ia} = 0.438 \frac{V_{an(peak)}}{I_{s_{rms}}} \frac{T_b}{2}. \tag{7}$$

The value of peak source voltage was derived from the rms source voltage stated in the assumptions which also determined the simulation inductance by using Eq. (5). For the 3 kW design utilizing a 24 kHz boost switch frequency, solving for L_{ia} in Eq. (7) results in a boost inductance value of 32.3 μH. This is a maximum L_{ia} because Eq. (7) determines a value of inductance to draw sufficient I_{srms} to supply rated load. Analysis of Eq. (7) indicates that a larger L_{ia} will result in a smaller I_{srms} that is insufficient for rated load.

2.1.3. OUTPUT CAPACITOR DESIGN

The output filter capacitor C_{dc} determines the output peak-to-peak ripple voltage. C_{dc} is determined using boost converter theory found in Ref. [1] combined with circuit simulation results. To determine capacitance, the current through the boost diode and the output voltage are analyzed. The spectrum of the current through the boost diode in Fig. 4 shows that the dominant harmonic component occurs at the frequency of the boost switch. The value of capacitance is found using the familiar circuit model I = C(dv/dt). Fig. 5 shows the boost diode current, output current, and output voltage waveforms used to determine C_{dc}. Assuming that the ripple current of the boost diode flows through C_{dc} and the average value of the diode current is the dc component being supplied to the load, the waveform data of Fig. 5 can be used to solve for capacitance using the capacitance definition above. Using I = C(dv/dt),

$$I = C\frac{dv}{dt} \approx C\frac{\Delta v}{\Delta t} \Rightarrow C_{dc} = \frac{I \cdot \Delta t}{\Delta v_{dc}} \approx \frac{\Delta Q}{\Delta v_{dc}}. \tag{8}$$

Using the simulation currents and voltage waveforms shown in Fig. 5, the approximations

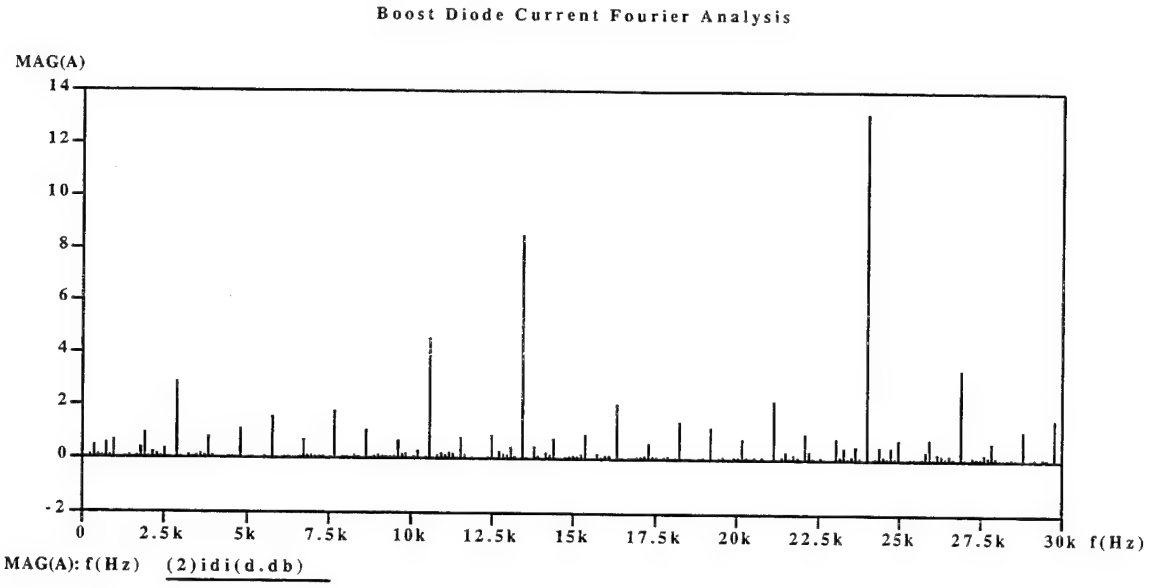


Fig. 4. Boost diode current in the frequency domain.

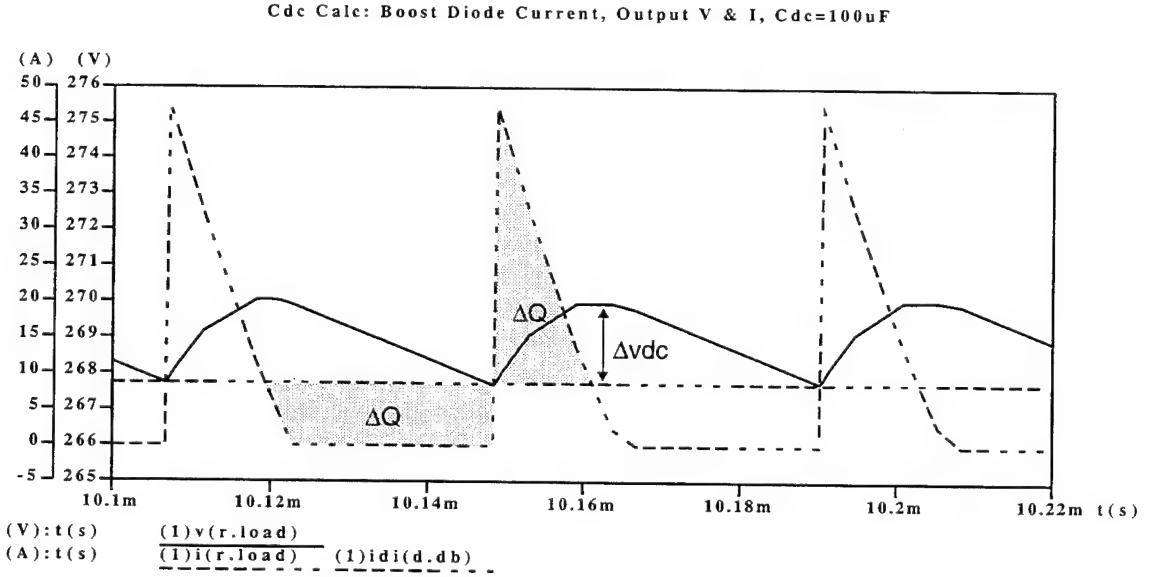


Fig. 5. Voltage and current waveforms used for C_{dc} graphical calculation.

in Eq. (8) are verified by finding C_{dc} to be equal to the simulation value:

$$C_{dc} = \frac{\Delta Q}{\Delta v_{dc}} = \frac{0.5 * 12.3\mu * 38}{2.3} = \frac{234\text{x}10^{-6}}{2.3} \simeq 100\ \mu\text{F}. \qquad (9)$$

This approximation method is used to identify the output capacitor value required

to attenuate the output voltage ripple produced by the rectifier. The full-bridge will contribute a 360 Hz component to the output voltage ripple. Fig. 6 illustrates the output voltage waveform in a longer time window than what is used in Fig. 5 with the C_{dc} =

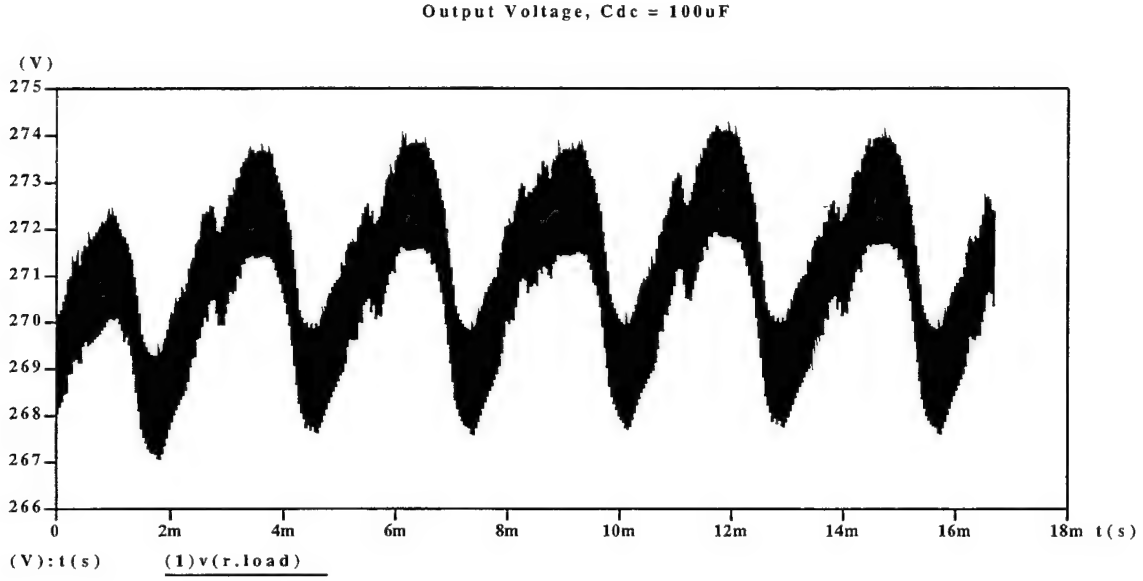


Fig. 6. Output voltage waveform with C_{dc} = 100 μF.

100μF. The dominant ripple harmonic shown expanded in Fig. 5 and the low frequency rectifier ripple component of approximately 7 $V_{pk\text{-}pk}$ seen in Fig. 6 must both be attenuated. In Eq. (9) ΔQ is constant and the dominant peak-to-peak ripple voltage is chosen to be attenuated to 0.27 V which is 0.1 % of the output voltage. Thus

$$C_{dc} = \frac{234\text{x}10^{-6}}{0.27} = 866\ \mu\text{F}. \tag{10}$$

Substitution of this value for output capacitance into the simulation attenuates the dominant output ripple component to the specified value of 0.27 V and also attenuates the low frequency harmonic component of the rectifier to approximately 1 $V_{pk\text{-}pk}$. This result is shown in Fig. 7 below.

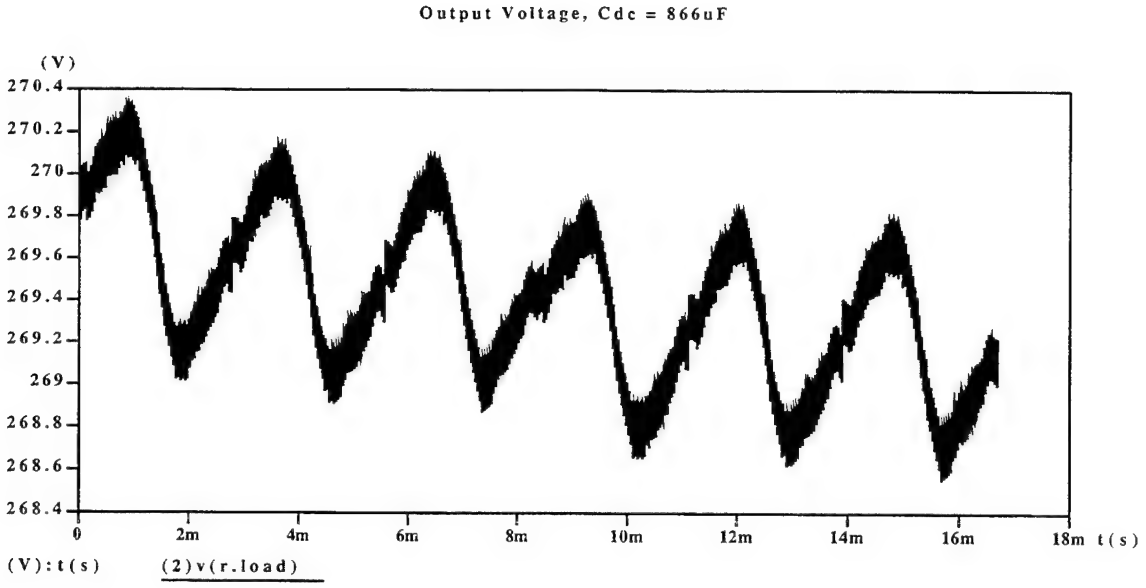


Fig. 7. Output voltage waveform with C_{dc} = 866 μF.

2.1.4. INPUT FILTER DESIGN

A single-phase analysis is used to design the input filter [4]. An equivalent circuit model for each phase of the input filter is shown in Fig. 8. $I_{s,n}$ is the source current composed of n harmonics and $I_{emi,n}$ is the n-th harmonic current generated by the boost circuit. L and C are the per-phase filter inductance and capacitance of the three-phase model. A current division analysis of the circuit found in Fig. 8 results in

$$I_{s,n} = - I_{emi,n}\left[\frac{\frac{1}{nj\omega C}}{nj\omega L + \frac{1}{nj\omega C}}\right]. \qquad (11)$$

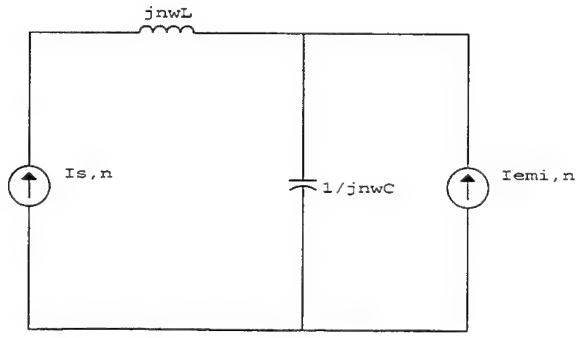


Fig. 8. Input filter per-phase equivalent circuit.

Rearranging Eq. (11) yields

$$LC = \frac{1}{(n\omega)^2}\left[\frac{I_{emi,n}}{I_{s,n}} + 1\right] \qquad (12)$$

and the product LC depends on the selected n-th harmonic frequency of ω where $\omega = 377$ rad.

To select an appropriate filter frequency, a frequency domain analysis of the simulated current reveals which frequency constitutes the dominant noise component. Figure 9 shows the magnitude spectrum of the simulated boost inductor current. Again the simulation is based on the circuit shown in Fig. 1 without the three-phase line filter. Analysis of this figure reveals the dominant harmonic at 23,940 Hz (n=399) with a magnitude of 10.2 A. Figure 9 also shows the 60 Hz fundamental component of the source to be approximately 22 A. Assuming the dominant harmonic created by the boost circuit must be attenuated to 3 % of the source fundamental, a similar assumption to that employed by Prasad in [2], lets $I_{s,n} = 0.66$ A. The input filter component values are then defined using Eq. (12) by,

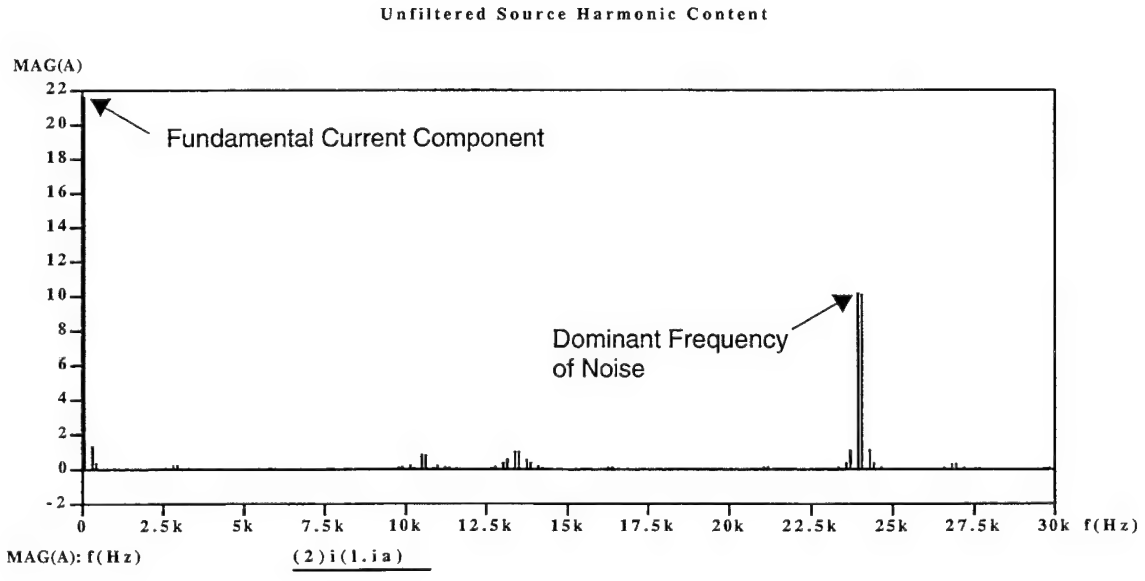


Fig. 9. Unfiltered ac source current spectrum.

$$LC = \frac{1}{(399 * 377)^2}\left[\frac{10.2}{0.66} + 1\right] = 7.27\text{x}10^{-10}. \quad (13)$$

Assuming that L = 66 μH, C is found to be 11 μF.

2.1.5. ACTIVE PFC DESIGN VERIFICATION

The completed three-phase boost active pfc design can be verified by a simulation of the ideal circuit including the input filter, boost inductor, and output capacitor in the simulation. The converter output voltage and current are assessed as well as the utility supply current and voltage waveforms. Fig.10a illustrates these waveforms. The output voltage is seen to be 270 Vdc, the output current is approximately 10 A, and the utility source current is nearly sinusoidal and in phase with the utility source voltage. Fig. 10b presents the spectral analysis of the utility source current confirming the attenuation of the harmonic components in the line current. The design goals are satisfied.

2.2. THREE-PHASE FULL-WAVE BRIDGE RECTIFIER DESIGN

The performance of the active pfc circuit is compared to the conventional three-phase full-bridge rectifier shown in Fig. 11. The design selects values for the output filter (L_f and C_f) and input filter (L_i and C_i). The load and bridge rectifier models are those used previously in the active pfc circuit design.

2.2.1. RECTIFIER OUTPUT FILTER DESIGN

The equivalent circuit for output filter design is shown in Fig. 12 [4]. Applying voltage division to Fig. 12, neglecting the load effect since Rl >> $1/\omega C_f$, the output voltage V_o can be expressed in terms of the input voltage V_i as,

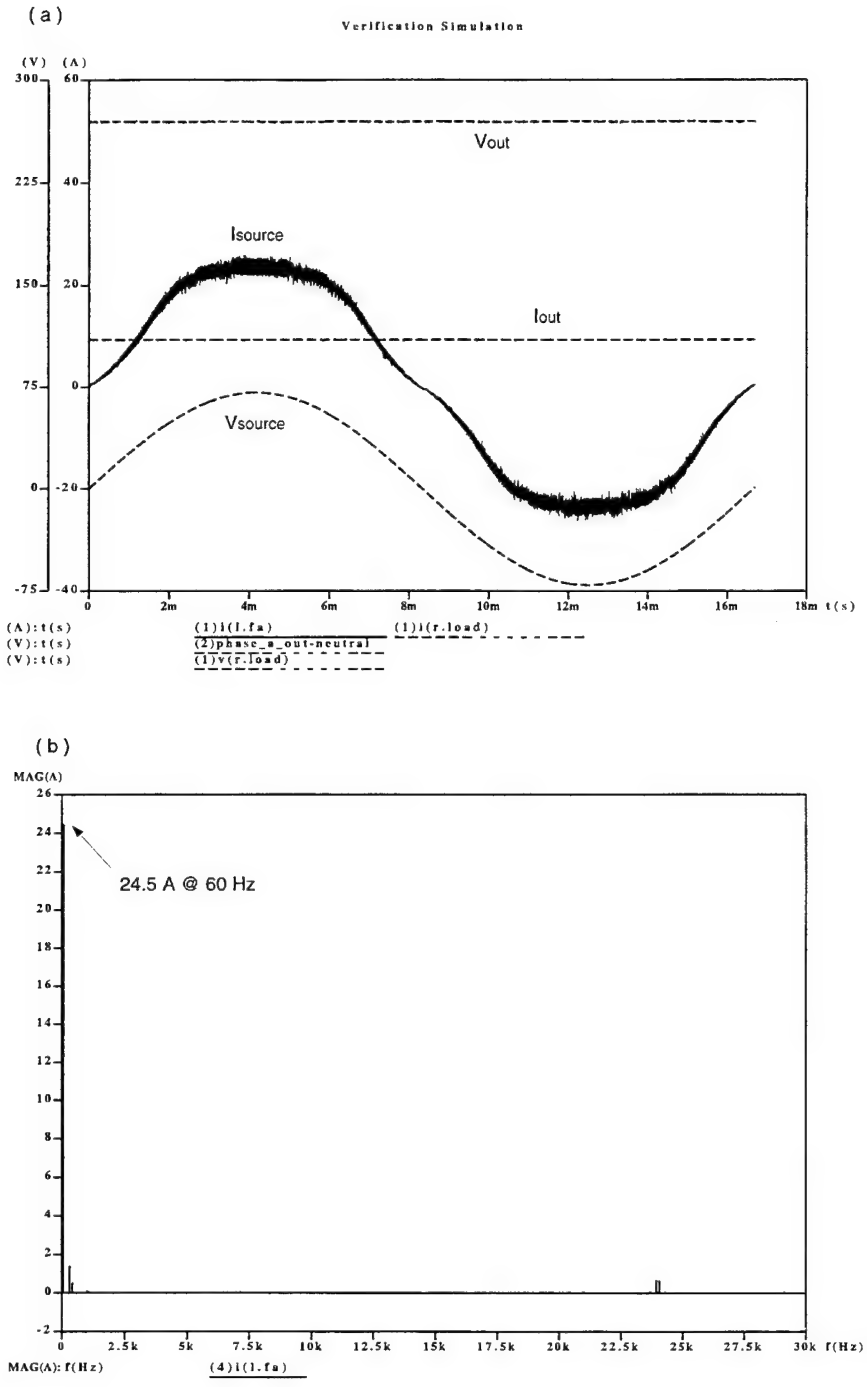


Fig. 10. (a) Simulated output voltage, output current, and filtered ac source current and voltage (phase A) waveforms for 3 kW active pfc design. (b) Filtered ac source current spectrum

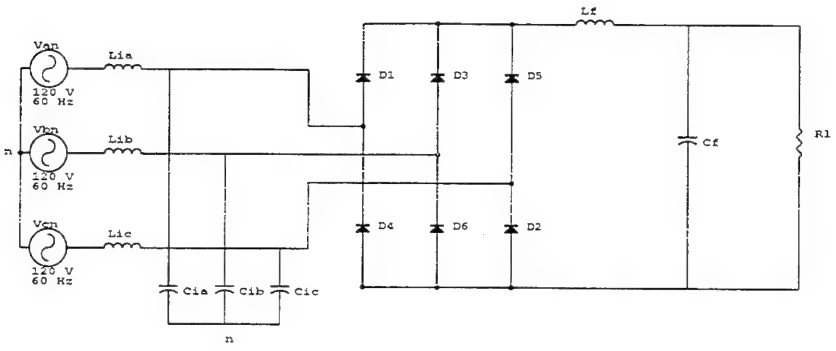


Fig. 11: Three phase full bridge rectifier with input and output filters.

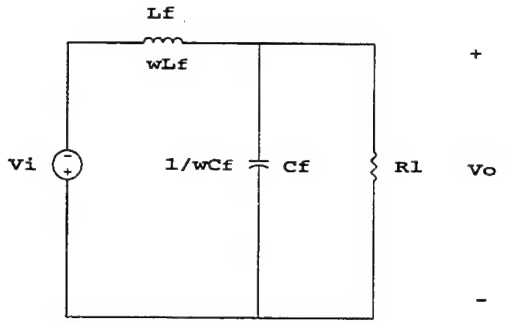


Fig. 12: Equivalent circuit for output filter design.

$$V_o = -\frac{\frac{1}{j\omega C_f}}{j\omega L_f + \frac{1}{j\omega C_f}} V_i. \tag{14}$$

Rearranging this equation yields,

$$\frac{V_o}{V_i} = \frac{1}{\omega^2 L_f C_f - 1}. \tag{15}$$

The results of a simulation of the circuit of Fig. 11 with the input and output filters removed are shown in Fig. 13. The node equations are located in Appendix A. The dominant output harmonic occurs at 360 Hz (six times the supply frequency) with an estimated magnitude of 16 V. For design of the output filter, the 360 Hz output component is required to have a magnitude of 2.8 V (1% of output voltage) and Eq. (15) yields $L_f C_f = 1.31 \times 10^{-6}$. Choosing $L_f = 1.03$ mH, then $C_f = 1250$ μF. The simulation results of the filtered rectifier

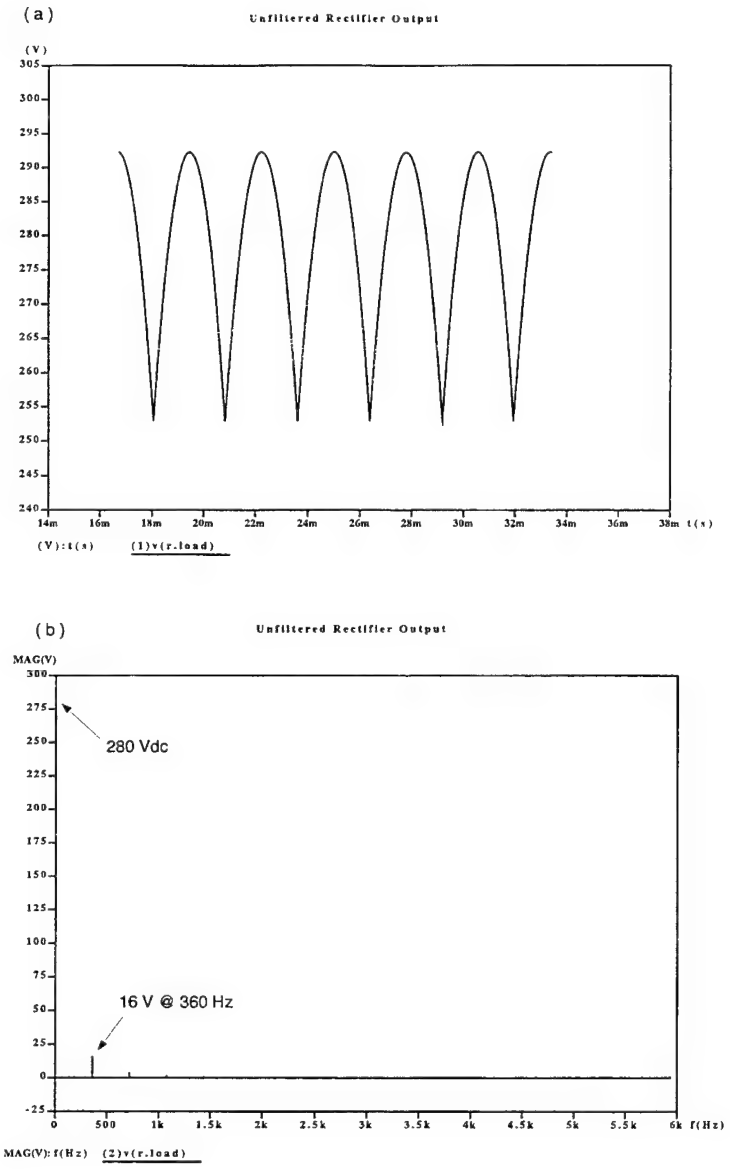


Fig. 13: (a) Unfiltered three-phase bridge rectifier output voltage waveform. (b) Unfiltered output voltage spectrum.

shown in Fig. 14 reveal that the resultant ripple is reduced to within the 1% ripple specification. The filtered output voltage is superimposed over the unfiltered output voltage in Fig. 14a to illustrate the attenuation. Comparing the frequency domain waveforms of Figs. 13b and 14b also illustrates the attenuation of the 360 Hz component. Fig. 15 shows the input current in both time and frequency domains before and after the output filter was added. The addition of the output filter is seen to contribute to the input current distortion.

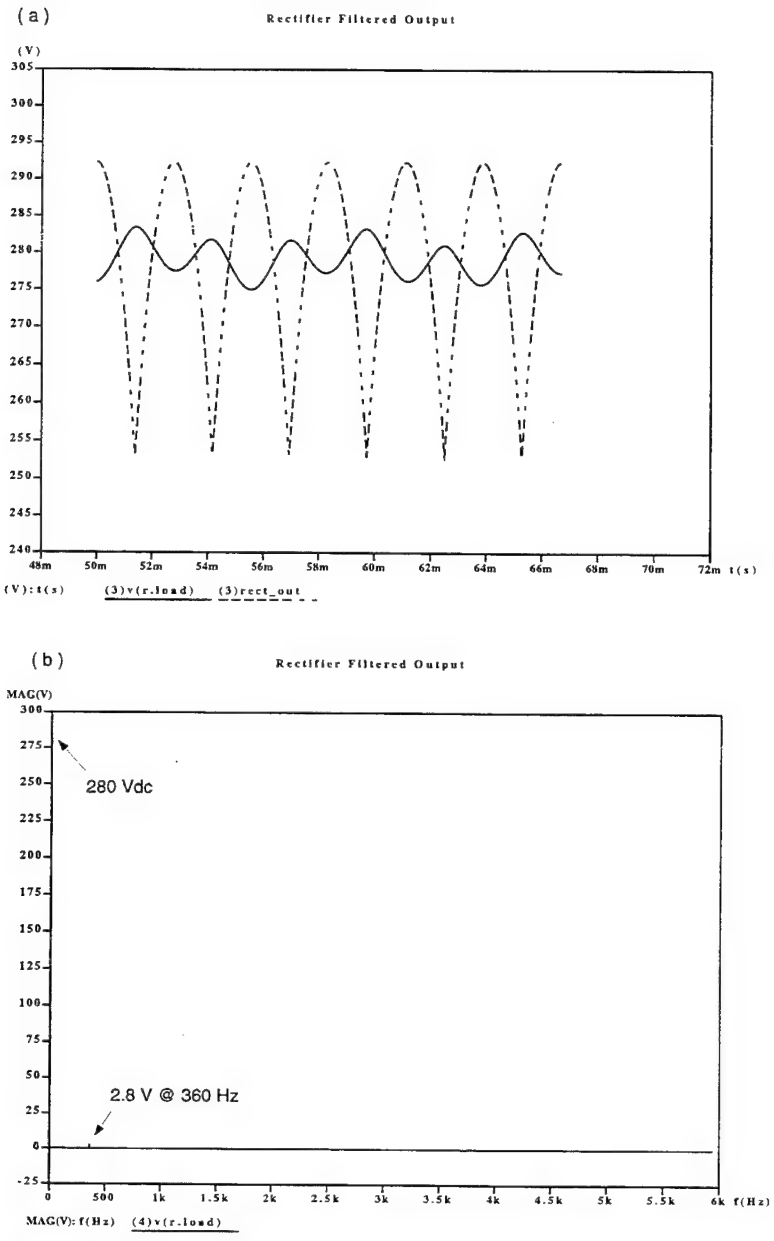


Fig. 14: (a) Filtered output voltage waveform superimposed over unfiltered output voltage waveform. (b) Filtered output voltage spectrum.

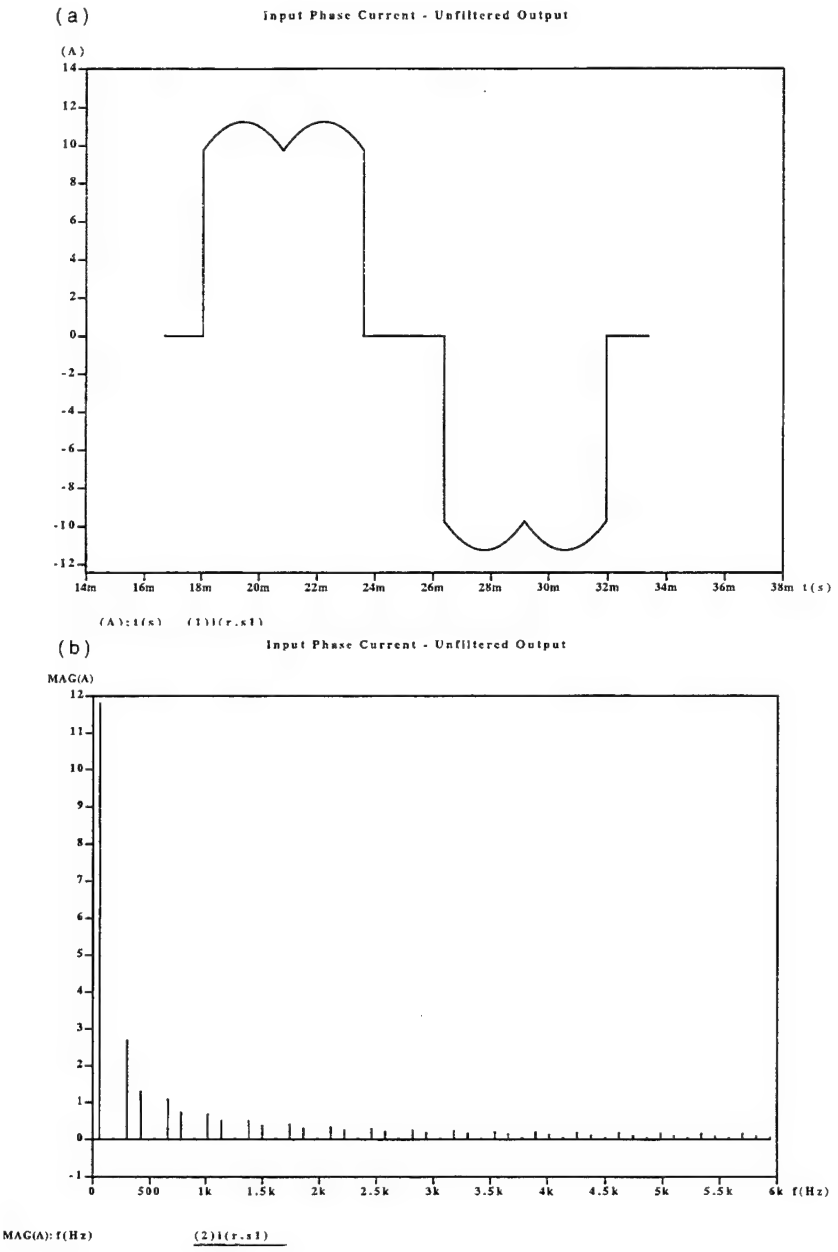


Fig. 15: (a) Input phase current waveform without output filter. (b) Input phase current spectrum without output filter. (c) Input phase current waveform with output filter. (d) Input phase current spectrum with output filter.

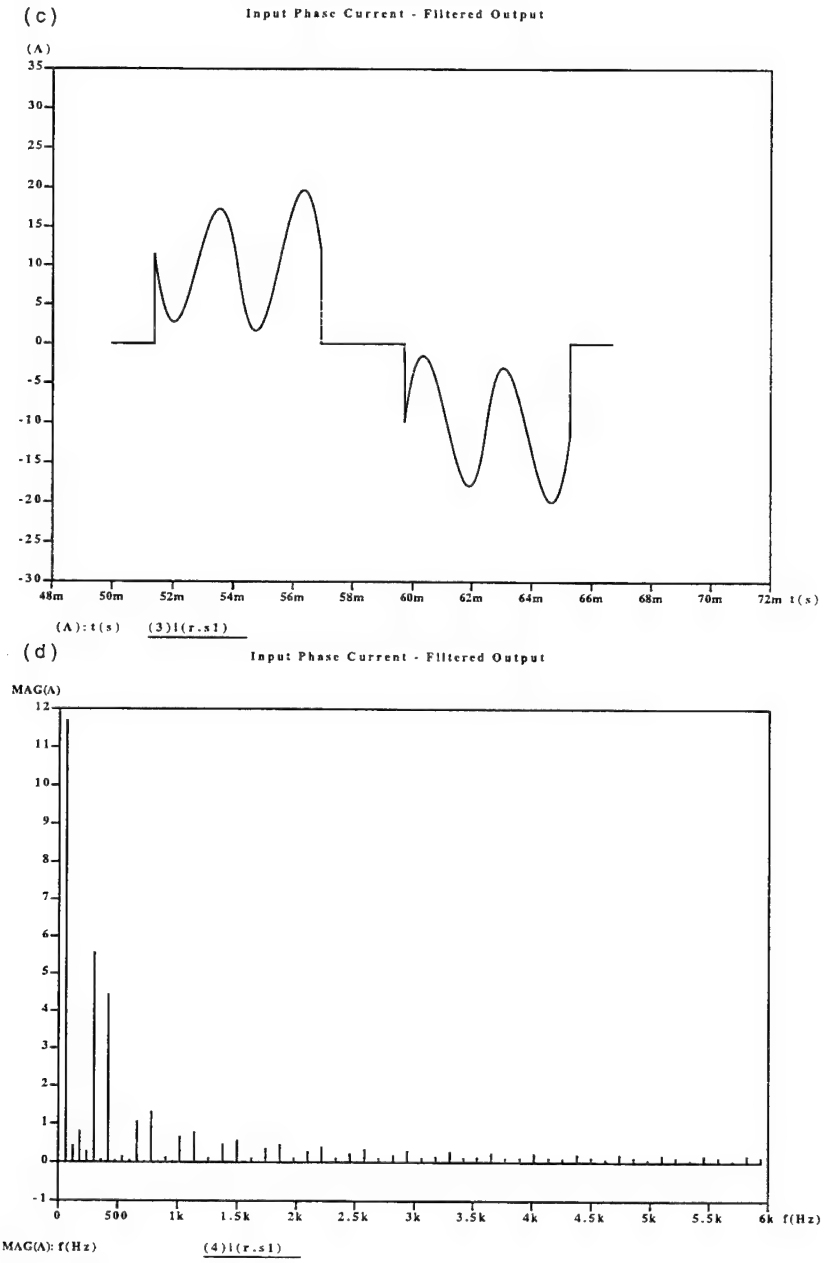


Fig. 15 (continued): (a) Input phase current waveform without output filter. (b) Input phase current spectrum without output filter. (c) Input phase current waveform with output filter. (d) Input phase current spectrum with output filter.

2.2.2. RECTIFIER INPUT FILTER DESIGN

The simulation results shown in Fig. 15 can be used to determine values for the input filter components. The input filter design method for the rectifier is the same design method used for the active pfc circuit described earlier. Fig. 15 reveals the dominant input current harmonic to be at 300 Hz. The magnitude of this harmonic current before the output filter was included in the simulation was 2.7 A, and after output filtering was included, it increased to 5.6 A. Selecting the dominant harmonic be attenuated to 2.7 A, which was its magnitude before output filtering was added, Eq. (12) results in

$$\mathrm{LC} = \frac{1}{(5 * 377)^2}\left[\frac{5.6}{2.7} + 1\right] = 8.65\mathrm{x}10^{-7}.$$

This corresponds to a filter cutoff frequency of

$$\frac{1}{\sqrt{\mathrm{LC}}} = \frac{1}{\sqrt{8.65\mathrm{x}10^{-7}}} = 1075\,\mathrm{rad} = 171\mathrm{Hz}$$

and the values of L and C that will implement this filter are too large to feasibly implement here. For example, selecting L = 66 μH (the value selected for the active pfc input filter) would select C = 13 mF. Thus the conventional full-wave bridge circuit that is compared to the active pfc circuit will not contain the input filter shown in Fig. 11.

CHAPTER 3
CIRCUIT FABRICATION ISSUES

The practical implementation of the active pfc design described in Chapter 2 requires some additional consideration of the circuit performance. As mentioned previously, the simulations assumed ideal component characteristics and did not consider circuit inefficiencies and deficiencies such as the destructive transient voltages seen by the boost switch. The practical implementation of the design will highlight these issues. The simulation results and subsequent design analysis identifies the component values required to satisfy the design specifications. However inductors are not components that are typically selected from inventory since they are typically application specific. For the experimental work discussed here, inductors were available that would satisfy the requirements of the input harmonic filter. The boost inductors however required fabrication and their design is presented in the following section. Snubber network design to manage the destructive transient voltages experienced by the IGBT boost switch is also described.

3.1. BOOST INDUCTOR DESIGN

The boost inductor design is based on commercially available ferrite cores [5]. The cores were E-type cores with $l_c = 0.107$ m, $A_c = 3.38$ cm^2, $\mu_c = 1745$, and B = 0.5 T

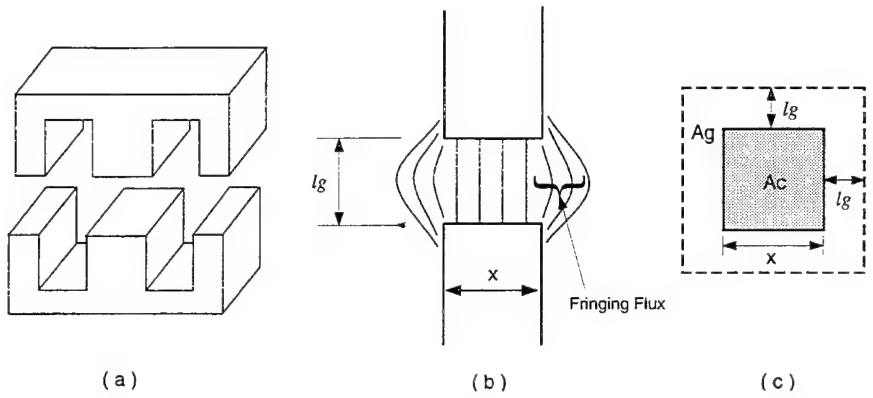


Fig. 16. (a) Magnetic core composed of twe E-type cores. (b)Fringing flux in the air gap. (c) Estimation of the air gap effective cross-sectional area.

where l_c is defined as magnetic path length of the core, A_c is the effective core area, μ_c is the permeability of the core, and B is magnetic flux density. The E-type core is shown in Fig. 16a.

The first step in the design process is to determine whether or not the core needs to be gapped. This can be determined by the familiar relationship $B = \mu H$ where H is magnetic field intensity. Under standard magnetic circuit analysis assumptions, this relationship can be approximated by

$$B = \mu \frac{Ni}{l_c} = \mu_0 \mu_c \frac{Ni}{l_c} \qquad (16)$$

where N is the number of wire turns, i is the current through the inductor, and μ_0 is the permeability of free space. The simulation results for the three-phase power factor correction design including the input and output filters, shown in Fig. 17, reveal the maximum inductor current to be 53 A. Solving Eq. (16) for the number of turns, N, it is found that for an ungapped core, the maximum amount of turns allowed (based on core properties and inductor current) would be less than 0.5 turns, which is not feasible. Thus a gapped core is required for this application.

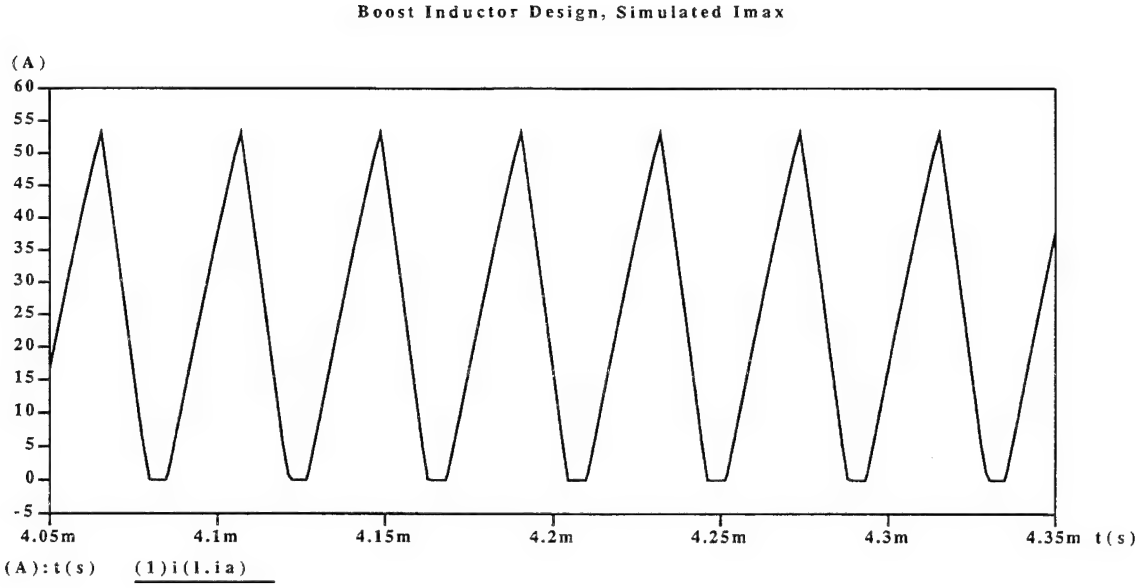


Fig. 17. Boost inductor current for inductor design.

Repeating this procedure assuming a gapped core with a gap length of 2.54 mm (chosen based on previous inductor design experience) the required inductor turns can be determined. The expression for magnetic flux density is now approximated as,

$$B = \frac{Ni}{\frac{l_c}{\mu_0 \mu_c} + \frac{l_g}{\mu_0}} \approx \frac{Ni}{\frac{l_g}{\mu_0}} . \qquad (17)$$

The approximation in Eq. (17) is valid provided the gap length is small compared to the magnetic length of the core and implies that most of the inductor energy is stored in the gap. Equation (17) is solved for N which will be the maximum allowable number of turns that will prevent core saturation and yields $N_{max} = 19$.

The next step in the inductor design uses the relationship

$$\lambda = NAB = Vt \qquad (18)$$

where λ is defined as flux linkage and will yield the minimum value of N. Vt is the maximum volt-time product across the inductor. The simulated inductor voltage is shown in Fig. 18. The volt-time product is estimated to be 125 V * 15μs = 1.9 mVs. In solving

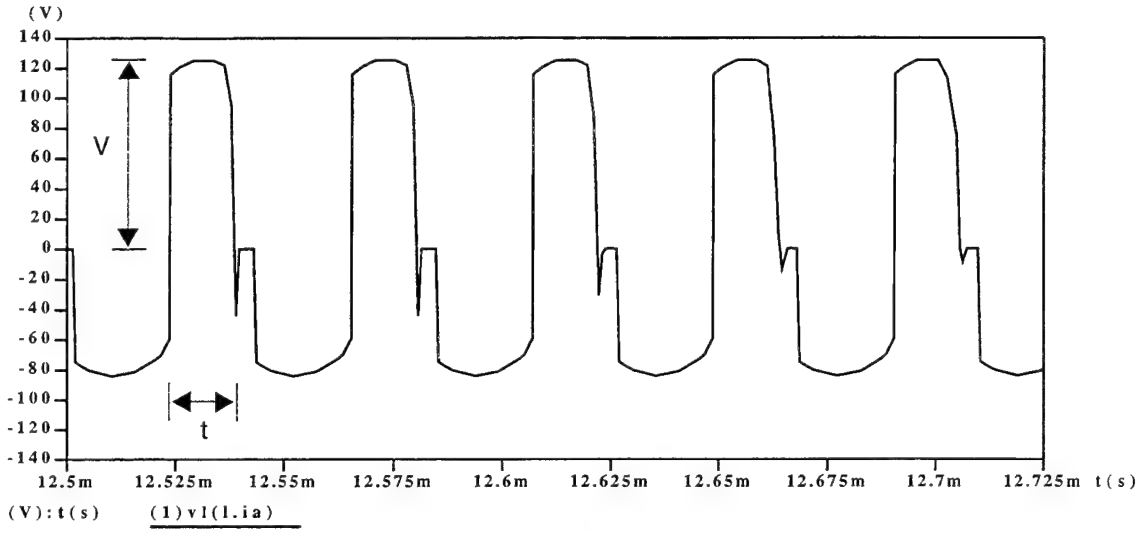


Fig. 18. Boost inductor maximum voltage for inductor design.

Eq. (18), the area of the gap, A_g, is used since most of the inductor energy is stored in the gap. Gap area is larger than the core area due to fringing. The fringing effect and gap area are illustrated in Fig. 16. The area of the core is normally square and using Fig. 16c, A_g is estimated as

$$A_g = \left(\sqrt{A_c} + 2l_g\right)^2. \qquad (19)$$

For this design, $A_g = 5.5\ cm^2$ and N_{min} is found to be 7.

For the specified current, volt-time product, and gap length, the valid range for N is determined as $N_{min} < N < N_{max}$. To find N for the desired inductance, the standard approximation is used:

$$L = \frac{\lambda}{i} = \frac{NAB}{i} = \frac{N^2 A_g \mu_0}{l_g}. \qquad (20)$$

Letting L = 30 μH, N is found to be 10.5, which is within the allowable range of turns. The inductors were wound, and were subjected to electrical characterization to determine equivalent series resistance (esr), Q-factor, and inductance as a function of frequency with

a bias current of 25 A. The bias current is a dc current supplied by the characterization equipment which also injects an ac signal into the inductor to measure inductance. The inductors were also biased up to 40 A (equipment limit) to ensure that they did not saturate. The frequency characterization plots for the three boost inductors subject to the 25 A bias are included in Appendix B. These figures show the inductance of each inductor to be 30 $\mu H \pm 0.75\ \mu H$ with an esr $< 30\ m\Omega$, and $Q \approx 150$ at 24 kHz which is the frequency of the boost switch and the fundamental frequency component value of the current through the boost inductor.

3.2. SNUBBER NETWORK DESIGN

The active pfc circuit of Fig. 1 was fabricated with the values defined in Chapter 2 and is illustrated in Fig. 19. The input voltage was gradually increased from zero volts while voltage across the boost switch was observed. The boost switch selected was a 600 V, 100 A IGBT. The IGBT signal is generated by an IGBT gate driver (FUJI Part No.

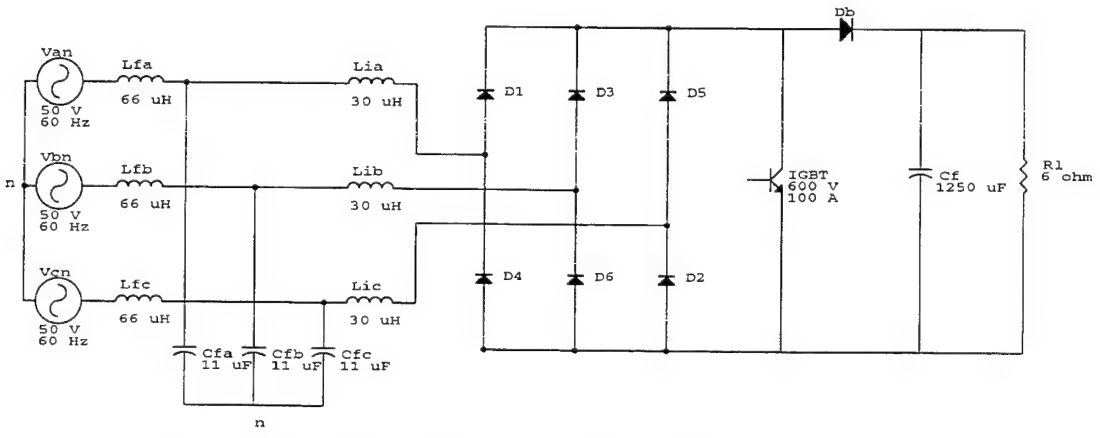


Fig. 19. Active pfc circuit as it was implemented without the snubber.

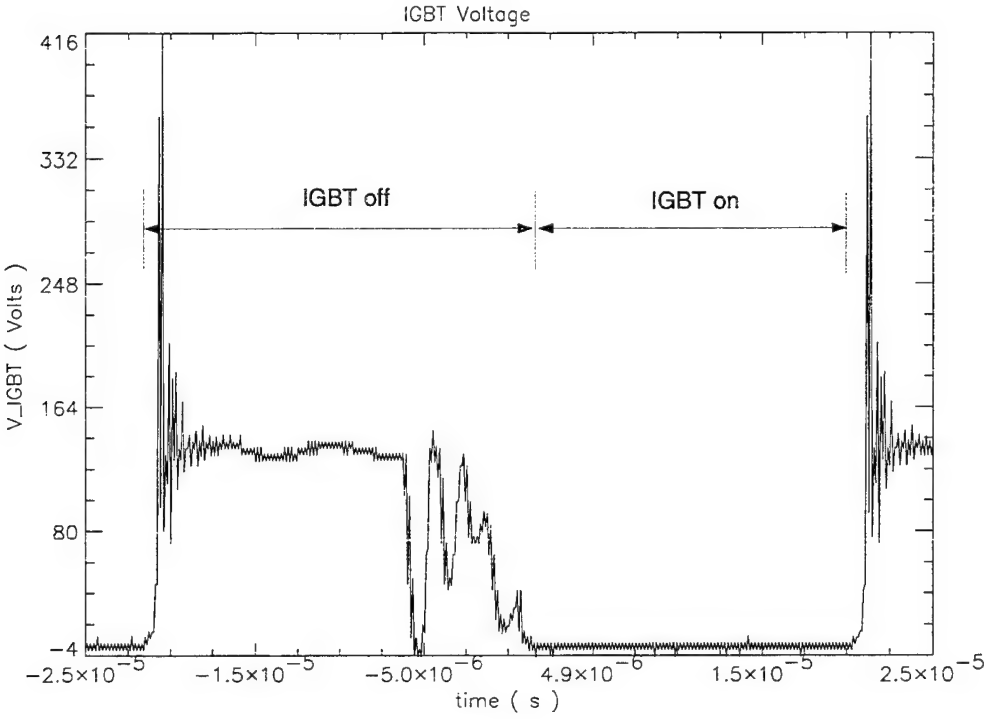


Fig. 20. Voltage across IGBT using recommended gate drive resistance, unsnubbered, and input phase voltage set to 25 V.

EXB840) controlled by a variable duty cycle function generator. The ideal nature of the simulation results does not permit any evaluation of turn-off spikes across the boost switch that are to be expected. Increasing the input phase voltage to 25 V per phase using the gate resistance recommended by the IGBT drive circuit data sheet results in turn-off spikes in excess of 400 V. This result is shown in Fig. 20. If the input voltage were increased to the 50 V per phase as required by the circuit specification, the spikes across the IGBT would damage the device. Fig. 21 shows two methods that can be used to decrease the voltage spike across the IGBT. Fig. 21a shows increased gate resistance in the IGBT circuit at device turn-off and Fig. 21b shows a turn-off snubber. The turn-off snubber is one recommended by the IGBT manufacturer [6] called a discharge restraint RCD snubber. Increasing the gate resistance at IGBT turn-off to lengthen the turn-off time does help

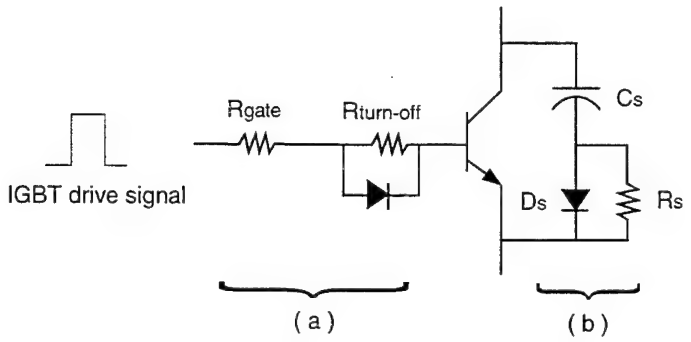


Fig. 21. (a) Turn-off slow down circuit. (b) Discharge-restraint RCD snubber.

somewhat. However as the gate resistance is increased, losses in the IGBT during turn-off may also damage the device. Snubber designs without increased gate resistance were investigated but the snubber losses experienced were too high. Thus a combination of slowed turn-off (increased gate resistance) with a turn-off snubber was adopted as the best approach for this type of application. Gate resistance was added to the turn-off by adding a Schottky diode / parallel resistor combination in series with the existing gate resistance as shown in Fig. 21a. This gate resistance manipulation reduced the boost switch voltage spike by 100 V which will increase turn-off losses in the IGBT, but decrease snubber losses.

To complete the snubber network design, it is necessary to find the value of effective inductance that is causing the spike. This can be estimated by applying $V = L(di/dt) \approx L(\Delta i/\Delta t)$ to the data shown in Fig. 22. This yields an effective inductance of approximately 6 μH. C_s is determined from [6] as

$$C_s = \frac{l * (I_o)^2}{(V_{cep} - E_d)^2} \qquad (21)$$

where l is effective main circuit stray inductance, I_o is collector current at IGBT turn-off,

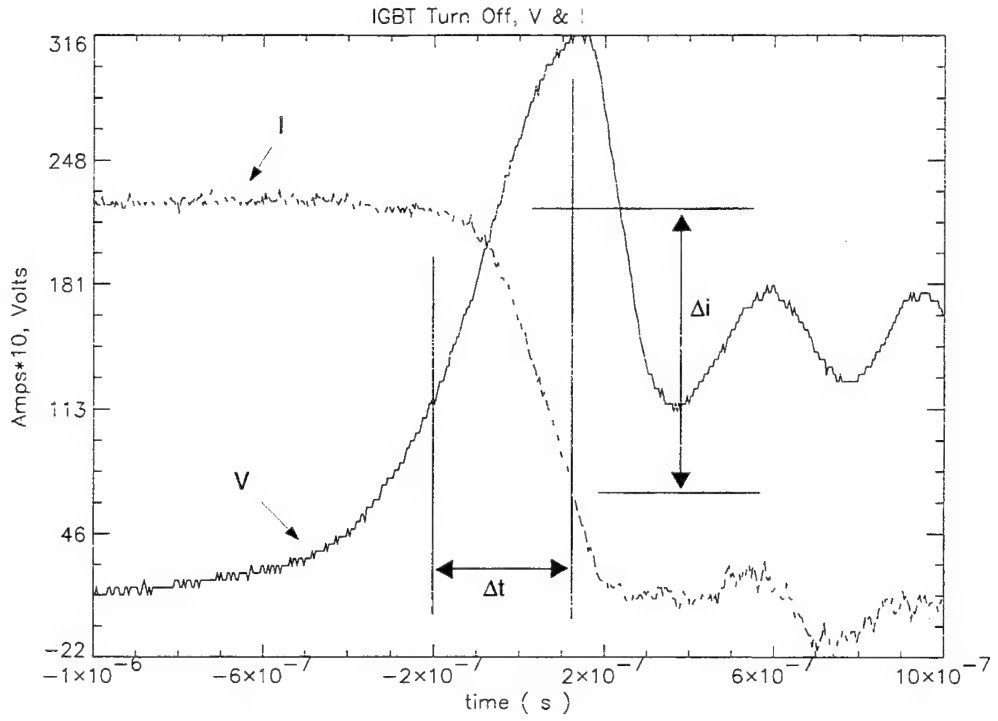


Fig. 22. Boost switch turn-off voltage and current for snubber design.

V_{cep} is the final value of snubber capacitor voltage, and E_d is the three-phase rectified voltage switched by the IGBT. R_s is found from the expression [6]

$$R_s \leq \frac{1}{6 * f * C_s}. \qquad (22)$$

where f is the switching frequency. R_s is chosen to ensure that the capacitor is sufficiently discharged before the next turn-off cycle. If R_s is chosen too small, the capacitor discharge will be too fast and will inject destructive, high peak currents into the IGBT. Solving Eqs. (21) and (22), yields $C_s = 0.1$ μF and $R_s \leq 69$ Ω. From Eq. (21) the turn-off spike with these parameter values should be reduced to approximately 220 V with input voltage set to 25 V per phase. This was verified experimentally for $C_s = 0.1$ μF and $R_s = 50$ Ω. Using these snubber values with an input phase voltage of 50 V, I_o becomes 42 A (for 1.6 kW

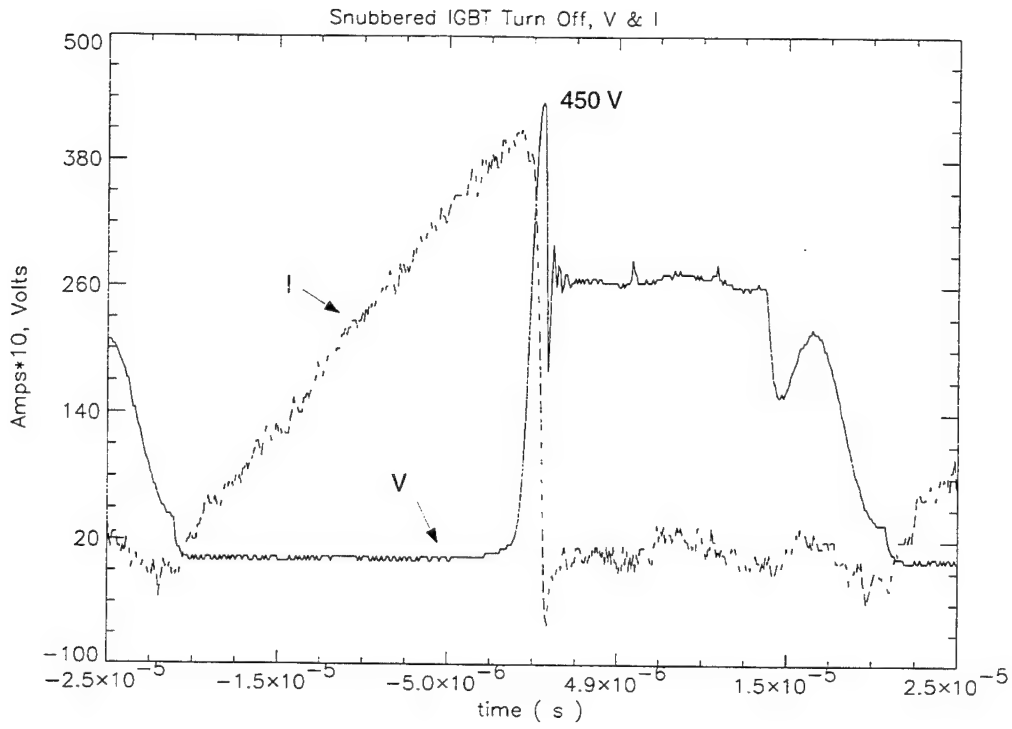


Fig. 23. Boost switch snubber performance verification.

load) and inserting these values into Eq. (21) predicts the voltage spike across the IGBT to be approximately 450 V. This result was confirmed experimentally and is shown in Fig. 23. Note that the pfc circuit is designed for 3 kW, but the load is now limited to 1.6 kW due to the stresses imposed on the boost switch. This power limit is the load value for which the temperature rises of the IGBT and snubber circuit stabilize within component temperature ratings.

CHAPTER 4
DISCUSSION OF EXPERIMENTAL RESULTS

The following sections present experimental results illustrating the performance of the three-phase boost active pfc rectifier and the conventional three-phase full-wave bridge rectifier.

4.1. THREE-PHASE BOOST ACTIVE PFC RECTIFIER RESULTS

The results in this section illustrate the performance of the active pfc circuit that was fabricated and tested. Oscilloscope data is presented for only the resistive load to illustrate circuit performance and provide a comparison to simulation results. Circuit power factor and efficiency measurements are presented for both the resistive and constant power loads and show that the constant power load did not affect the circuit performance.

4.1.1. ACTIVE PFC CIRCUIT WITH RESISTIVE LOAD

Table 1 shows the power measurements obtained for the active pfc circuit with a 1.6 kW resistive load. Total circuit efficiency from utility (480 Vac) to load is 76 % with a unity pf rating. Neglecting the supply transformer, the efficiency of the boost circuit is 81% at near unity pf. Figs. 24 - 37 illustrate the active pfc circuit performance at various circuit locations. Fig. 24 shows the current through and the voltage across the boost induc-

Table 1: Power and pf measurements for active pfc circuit with a resistive load.	
Parameter (units)	Value
Utility pf	1.000
Utility power (W)	2116
Transformer secondary pf	0.988
Transformer secondary power (W)	1993
Output power (W)	1615
Overall Efficiency (%)	76

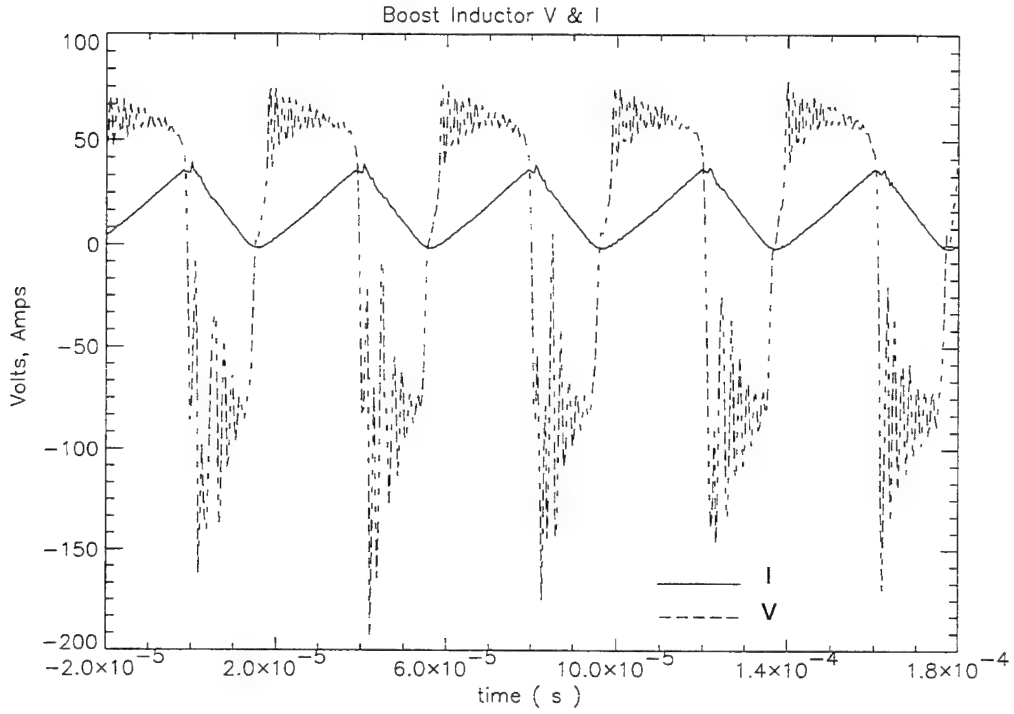


Fig. 24. Voltage across and current through boost inductor l_{ia}.

tor L_{ia}. This result confirms that the boost inductor current is discontinuous as designed and the inductor remains unsaturated. These waveforms resemble the simulation results of Figs. 17 and 18 although the V and I magnitudes are different as a result of a smaller actual load than that used in the simulation. The simulation waveforms show the maximum V and I to be 125 V and 53 A respectively and the experimental values are 68 V

and 40 A. The boost inductor current observed for 20 ms illustrates the presence of the 60 Hz fundamental component before input line filtering and this result is presented in Fig. 25.

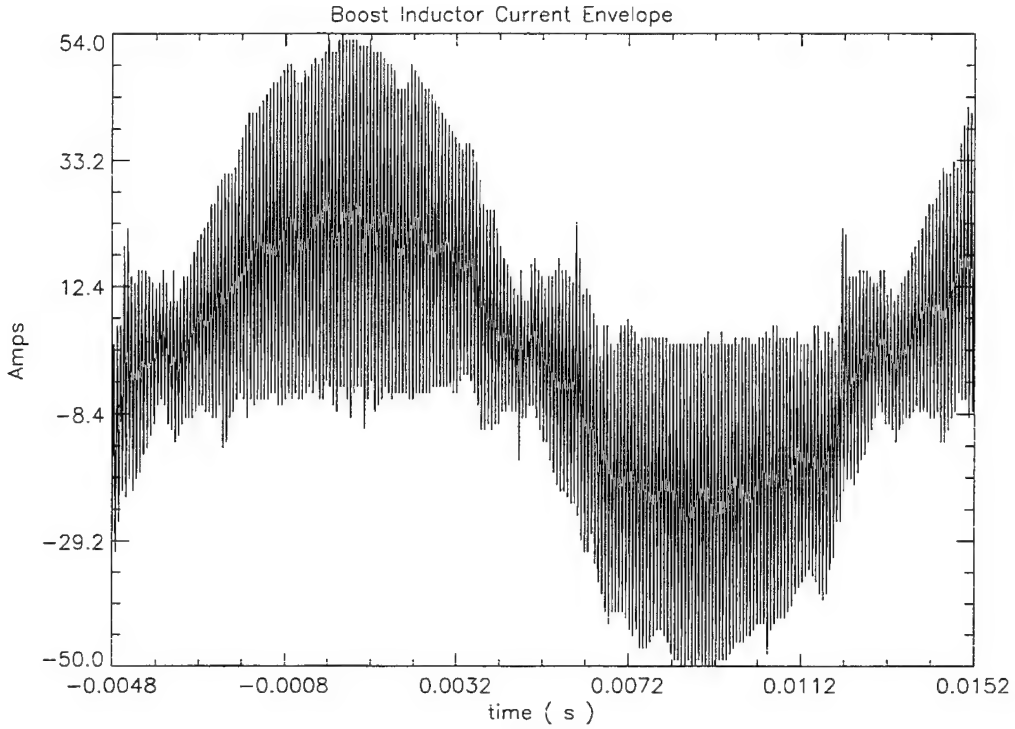


Fig. 25 Boost inductor current envelope.

Figs. 26 and 27 show the waveforms measured at the locations of the power meter where power factor was determined. The source voltage and current waveforms are contained in Fig. 26 and the transformer secondary voltage and current waveforms are in Fig. 27. Both of these figures show that the current is nearly sinusoidal after input filtering, as is apparent in the simulation results of Fig. 10. Although some noticeable distortion is evident in Figs. 10, 26, and 27 , the current is generally in phase with the voltage for unity displacement power factor and sufficiently sinusoidal for the power meter to read near unity power factor on both the transformer secondary and unity at the utility interface (transformer primary).

The corresponding spectra of the utility and transformer secondary currents are

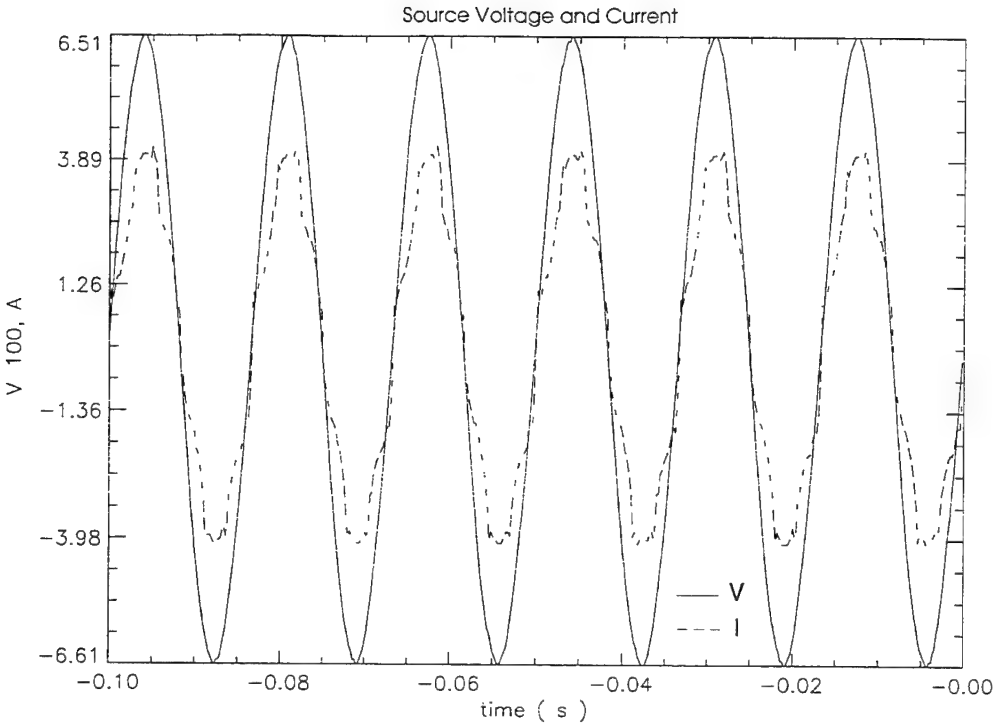


Fig. 26. Utility line - line voltage and phase current.

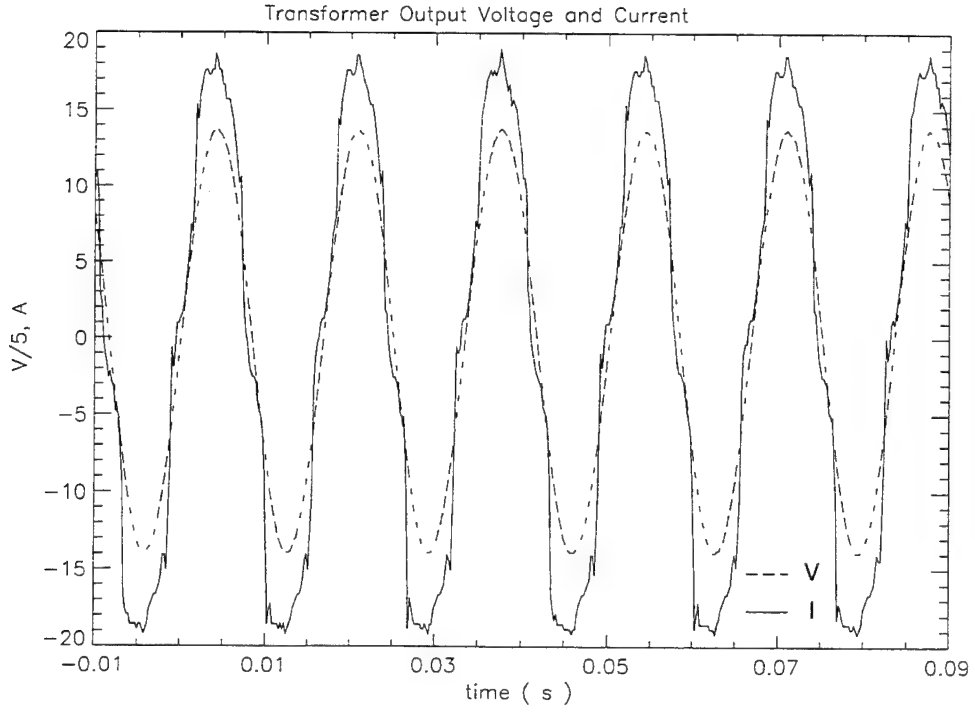


Fig. 27. Transformer secondary line - neutral voltage and phase current.

shown in Figs. 28-31. Figs. 29 and 31 show the spectra from dc to 40 KHz and Figs. 28 and 30 expand the spectra from dc to 1 KHz. Studying Figs. 28 and 29, the dominant harmonic in the transformer secondary is seen to be from the rectifier which contributes

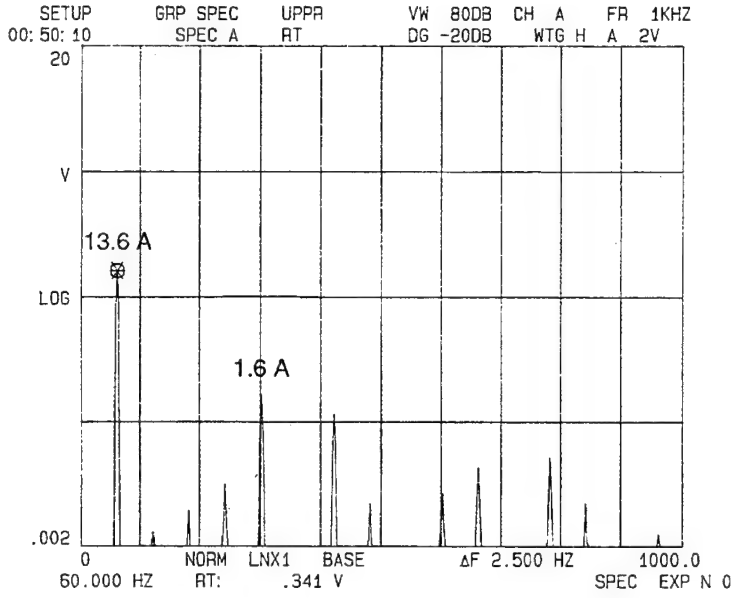


Fig.28. Transformer secondary current spectrum up to 1 Khz. Y axis is 0.025 amps/ volt.

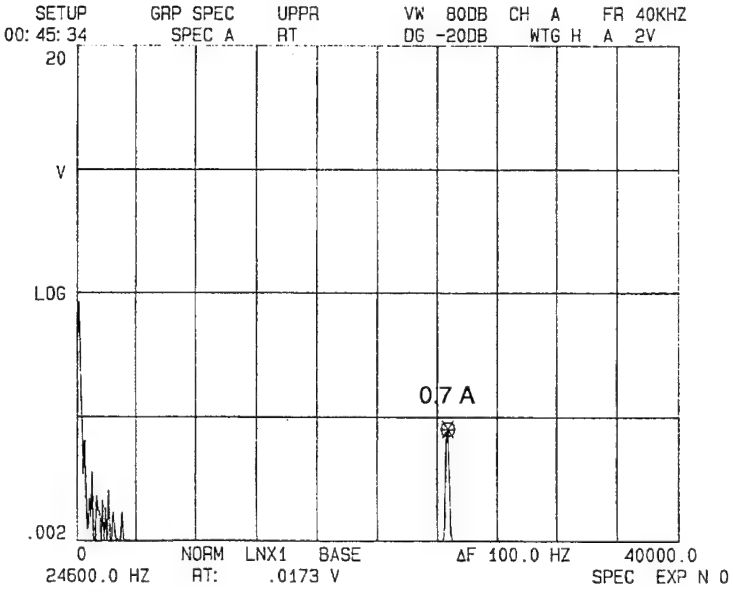


Fig. 29. Transformer secondary current spectrum up to 40 Khz. Y axis is 0.025 amps/ volt.

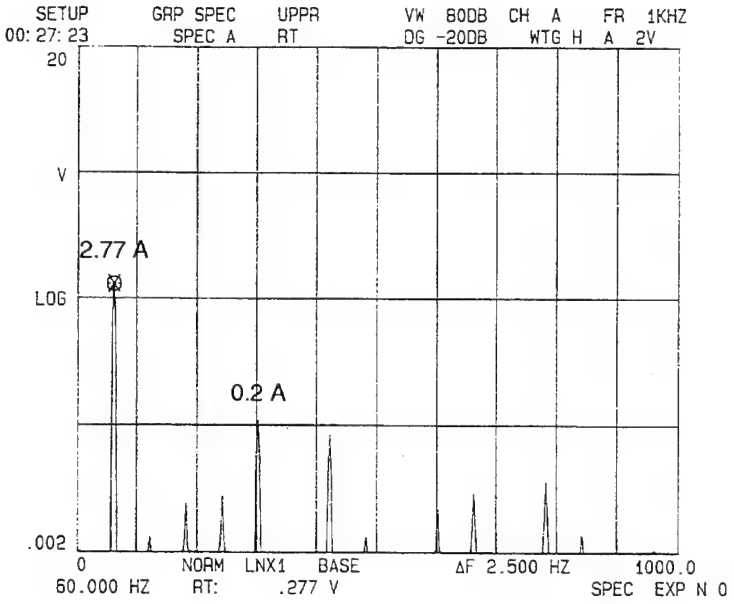


Fig. 30. Utility current spectrum up to 1 Khz.
Y axis is 0.1 amps/ volt.

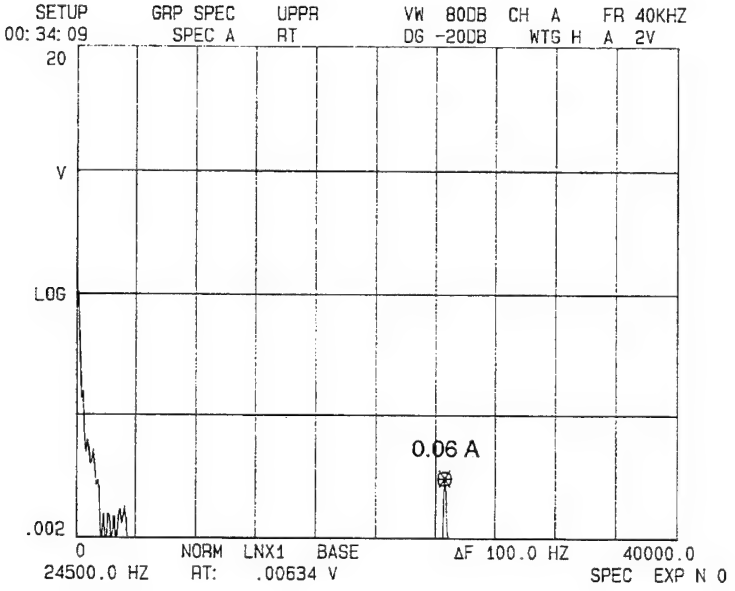


Fig. 31. Utility current spectrum up to 40 Khz.
Y axis is 0.1 amps/volt.

approximately 1.6 A at 300 Hz and the harmonic contributed from the boost circuit is measured to be 0.7 A at 24.6 KHz which is 5% of the fundamental 60 Hz component of

13.6 A. This is expected since the input filter frequency was chosen to attenuate the harmonics of the boost circuit and these results coincide with the dominant harmonic frequencies analyzed in Chapter 2. The original goal of the input filter design was to attenuate the boost switch frequency component to 3% of the fundamental at the utility source. Figs. 30 and 31 show that the transformer contributed to the input filtering in that the boost switch frequency component (0.06 A at 24.5 KHz) visible to the utility is 2.2% of the fundamental 60 Hz component of 2.77 A. Thus the combined effect of the isolation transformer and the input filter have met the design goal of attenuation of the boost switch frequency components.

The 270 Vdc output voltage waveform measured at the resistive load can be seen in Fig. 32. The spikes are a result of the transient associated with the boost switch turn-off

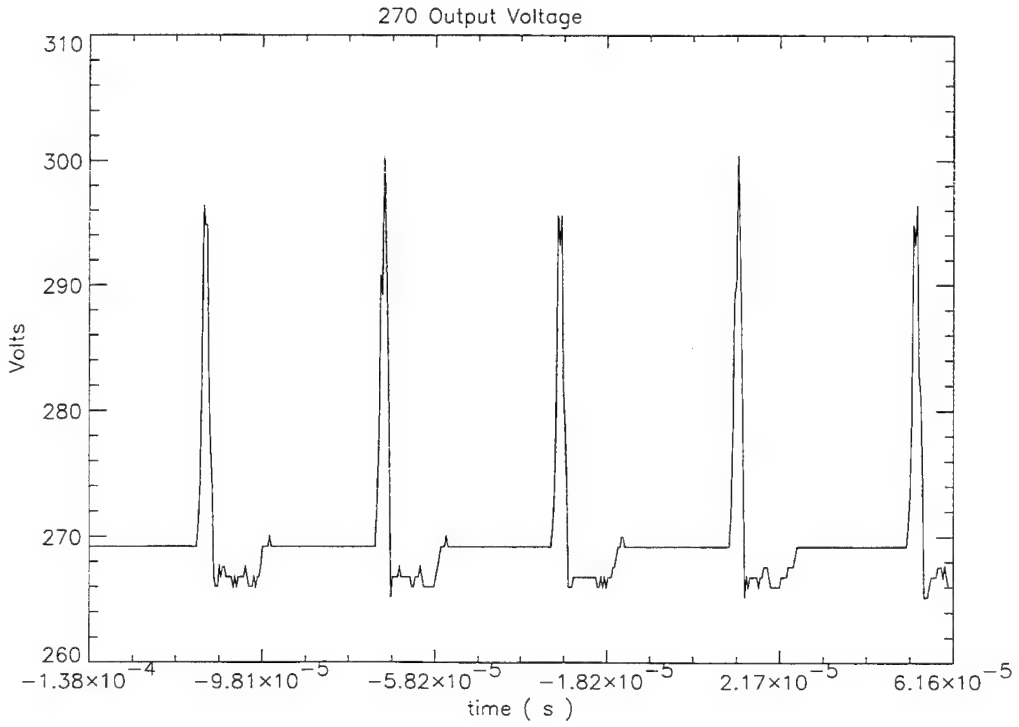


Fig. 32. Measured load voltage with 1.6 kW resistive load.

being passed to the load through the boost diode. They coincide with the transient voltage spikes across the boost switch except at a lesser magnitude due to some attenuation associated with the output capacitor. Additional output filtering or possibly a soft switching resonant circuit topology would be required to reduce or eliminate these spikes.

To complete the experimental assessment of the operating circuit, the voltage and current associated with the boost switch are considered. As mentioned earlier, the efficiency of the boost pfc circuit without the transformer is 81%. A majority of the losses associated with this efficiency can be attributed to the boost switch losses quantified by IGBT conduction and switching losses and snubber network losses required to absorb the destructive energy during switch turn-off.

Figs. 33 - 37 show some results of the voltage across and the current through the IGBT. Fig. 33 shows one complete IGBT off-on cycle, Fig. 34 and 35 show expanded views of the turn-on and turn-off phases, and Fig. 36 shows the IGBT when it is on. These results characterize the IGBT losses. Total switch power loss can be expressed as the sum of the switching losses (turn-on and turn-off) and conduction loss averaged over one switch on-off cycle. Switching loss can be approximated by

$$P_s = 0.5 V_o I_{avg} f_s [t_{on} + t_{off}] \qquad (23)$$

where V_o is the output voltage being switched, I_{avg} is the average conducted current, f_s is the switch frequency, t_{on} is the turn-on time of the switch, and t_{off} is the switch turn-off time [1]. Figs. 34-36 reveal the IGBT turn-on time to be 0.6 μs, turn-off time to be 0.8 μs, and the average conducted current to be approximately 20 A. The calculated switching loss based on these measurements is 90 W.

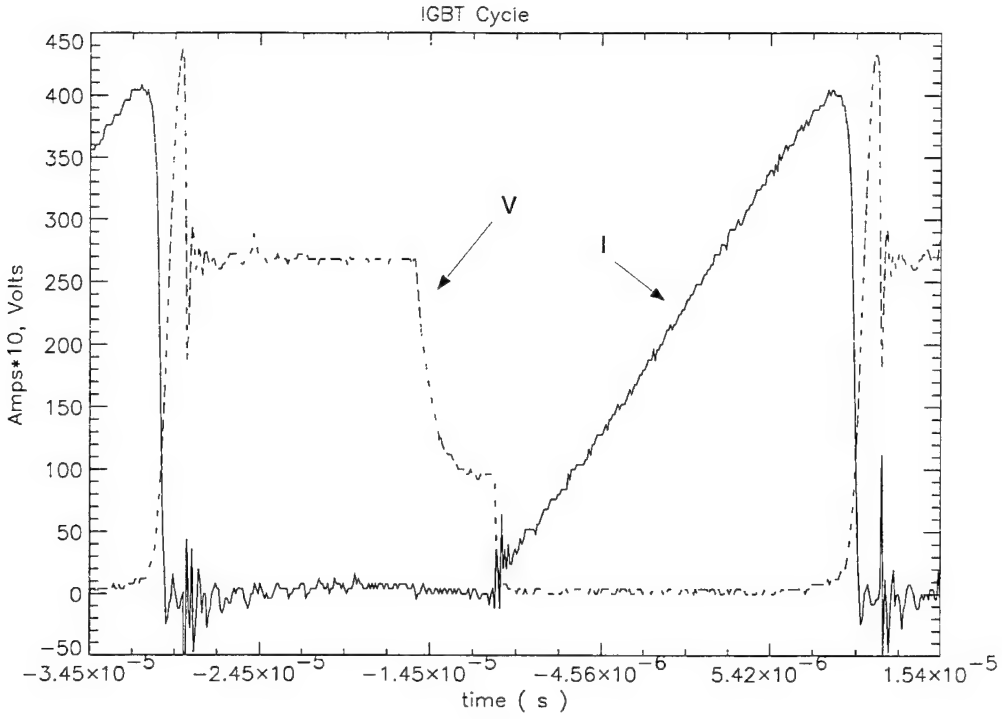


Fig. 33. Voltage across and current thru IGBT - Complete off - on cycle.

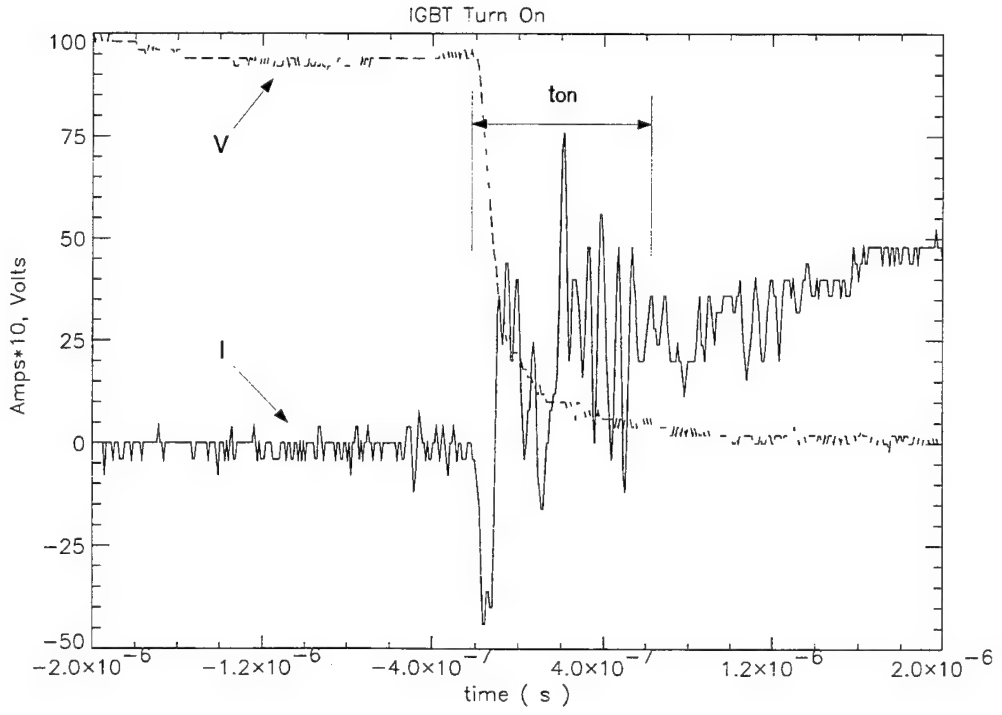


Fig. 34. Voltage across and current through IGBT during switch turn-on.

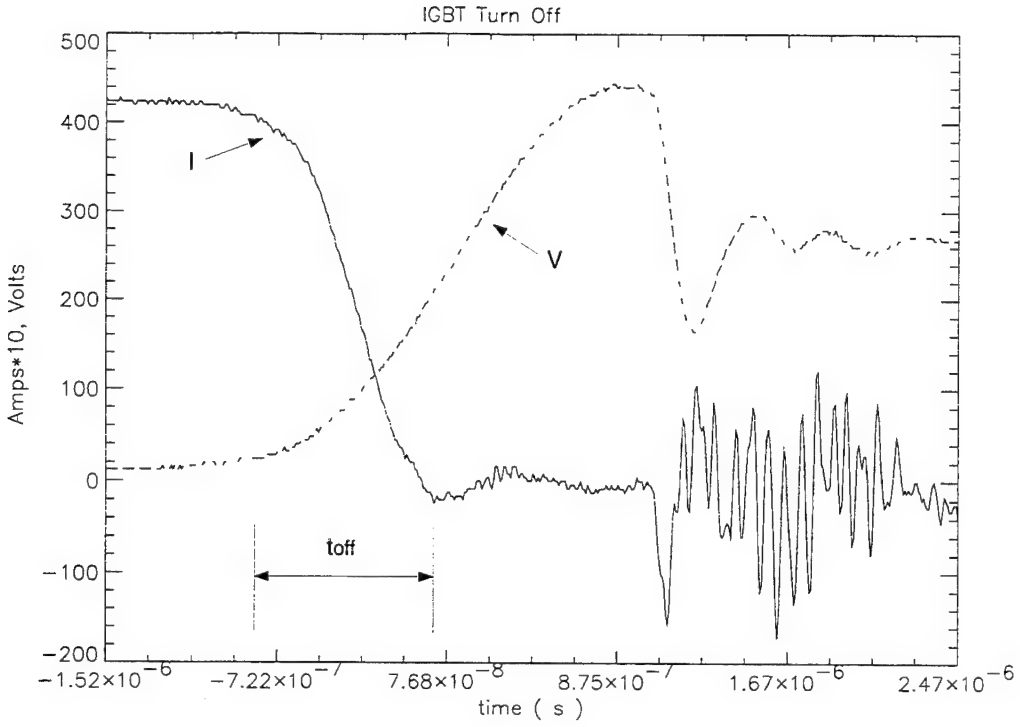


Fig. 35. Voltage across and current through IGBT during switch turn-off.

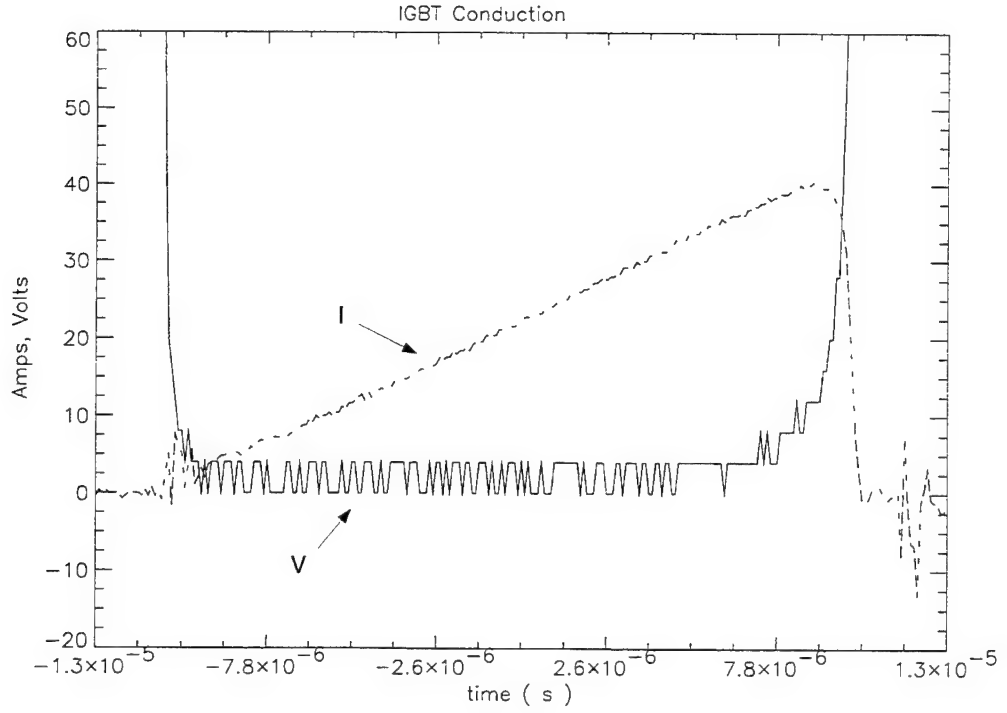


Fig. 36. Voltage across and current through IGBT during switch on.

Conduction losses can be approximated by

$$P_c = V_{on} I_{avg} D \tag{24}$$

where V_{on} is the IGBT on-time voltage drop, I_{avg} is the average conducted current, and D is the duty cycle of the switch. V_{on} = 2.5 V and I_{avg} = 20 A are measured from results found in Fig. 36, and D is approximately 0.5. These measurements provide an expected conduction loss estimate of 25 W. Thus the approximate total loss in the IGBT is 115 W.

The power loss dissipated by the snubber circuit during IGBT turn-off is also significant. Most of the snubber loss occurs in the snubber resistor. Fig. 37 shows the voltage across and current through the IGBT and voltage across the snubber resistor. The average snubber loss is typically estimated as

$$PRS = \frac{l I_o^2 f}{2} \tag{25}$$

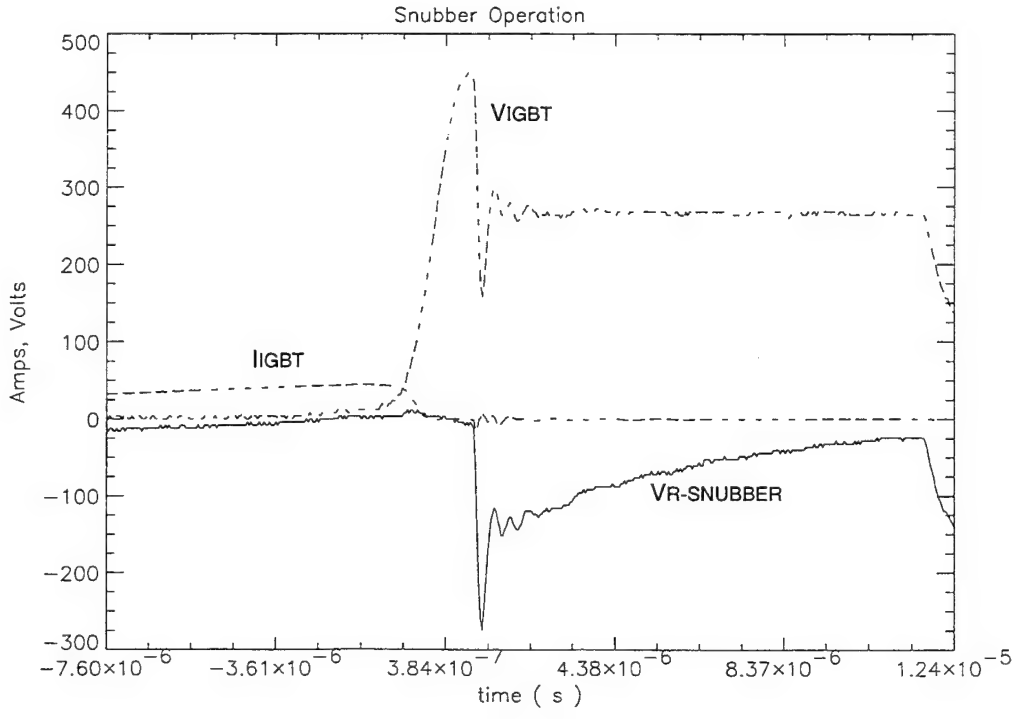


Fig. 37. Current through and voltage across IGBT and voltage across snubber resistor during IGBT turn-off.

where l is the effective stray inductance causing the transient, I_o is the IGBT collector current at turn-off, and f is the switch frequency [6]. The measured I_o (Fig. 35) is approximately 42 A and l, from the snubber design, is 6 μH. The average turn-off snubber power loss is then ≅ 127 W.

The total loss associated with the boost switch is 242 W representing both IGBT and snubber losses. This accounts for (242 / 378 * 100) = 64 % of the measured losses in the active pfc circuit (see Table 1). The remaining losses are dissipated in the boost diode, boost inductors, rectifier diodes, and filter components.

4.1.2. ACTIVE PFC CIRCUIT WITH CONSTANT POWER LOAD

Table 2 shows the power measurements taken from the active pfc circuit loaded with a 1.6 kW constant power load. Total circuit efficiency from utility to load is 73 % with unity pf. Neglecting the transformer, the efficiency of the boost circuit is 78 %. Note that the utility pf remains at unity. This illustrates the insensitivity of the active pfc rectifier to the load characteristics.

Table 2: Power and pf measurements for active pfc circuit, constant power load.

Parameter (units)	Value
Utility pf	1.000
Utility power (Watts)	2173
Transformer secondary pf	1.000
Transformer secondary power (Watts)	2024
Output power (Watts)	1580
Overall Efficiency (%)	73

4.2. THREE-PHASE FULL-WAVE BRIDGE RECTIFIER RESULTS

The performance of a three-phase full-wave bridge diode rectifier is presented for comparative purposes. Oscilloscope data was obtained for the resistive load to illustrate circuit performance and provide representative results. Power measurements were obtained for both the resistive and constant power loads to determine circuit power factor and efficiency.

4.2.1 RECTIFIER WITH RESISTIVE LOAD

The power measurements taken from the conventional rectifier circuit loaded with the same 1.6 kW resistive load used for the active pfc circuit are presented in Table 3. The efficiency of the rectifier circuit from utility (three-phase 120 Vac) to load was 97 %. The utility output voltage and current waveforms, where power factor was measured, is shown in Fig. 38. The distortion and phase shift evident in this result is quantified by the low power factor rating found in Table 3. The spectrum of the utility current waveform (Fig. 38) is shown in Fig. 39 and resembles the spectrum predicted by simulation results found in Fig. 15d in that the dominant harmonic is located at 300 Hz in both spectra. However the experimental dominant harmonic magnitude of Fig. 39 is higher with respect to the 60

Table 3: Power and pf measurements for full-wave rectifier, resistive load.

Parameter (units)	Value
Utility pf	0.78
Utility power (Watts)	1745
Output power (Watts)	1699
Overall Efficiency (%)	97

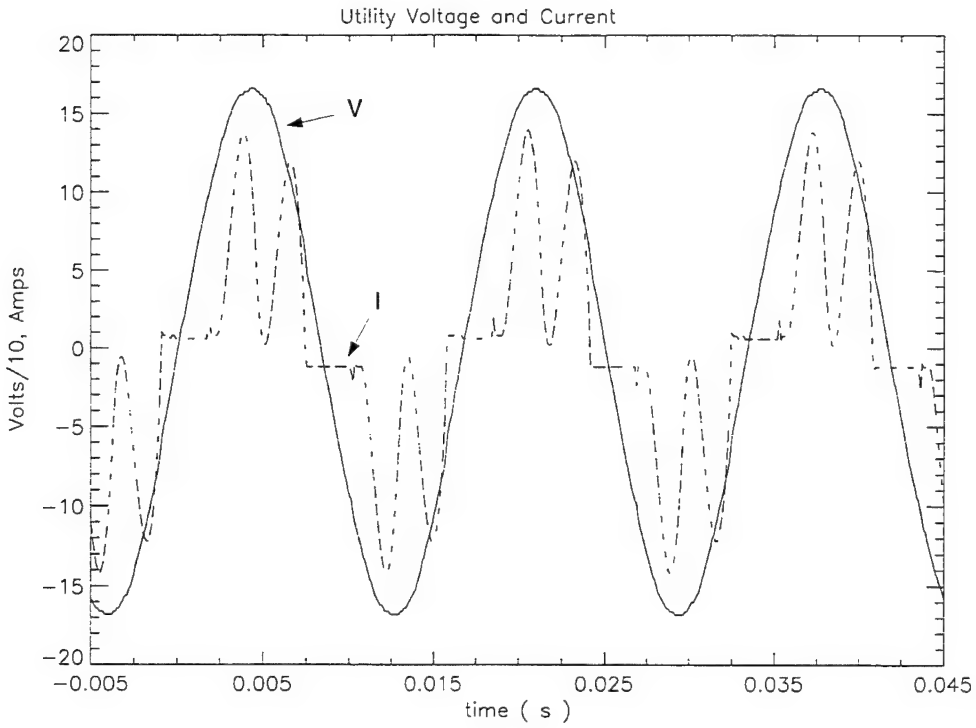


Fig. 38. Utility voltage and current into 3-phase bridge rectifier.

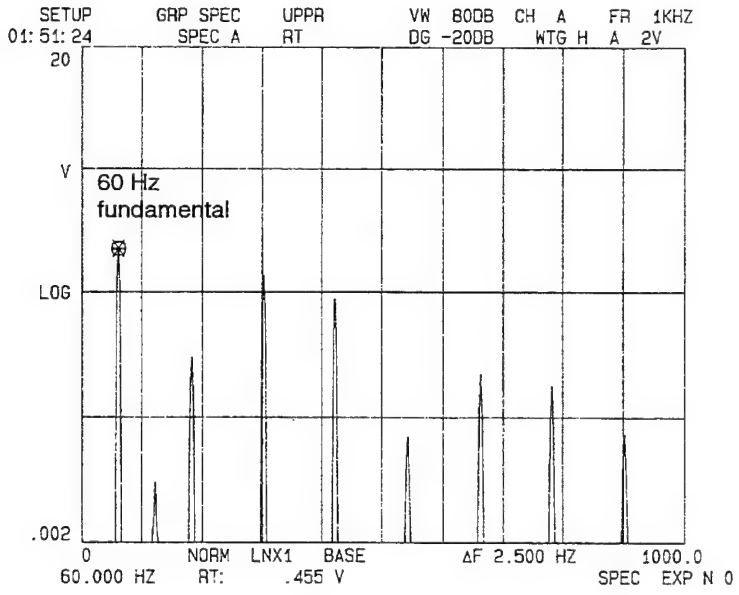


Fig. 39. Utility current spectrum up to 1 khz.
Y axis is 0.1 amps/volt magnitude

Hz fundamental component than the simulation results (Fig. 15d) predicted. The simulation results predicted the ratio of the 300 Hz harmonic magnitude to the 60 Hz fundamental magnitude to be approximately 0.48 and the measured ratio is approximately 0.66.

Fig. 40 shows the output voltage ripple on the rectified voltage. The corresponding spectrum is shown in Fig. 41. Note that the 360 Hz component has been attenuated to a magnitude of 1.5 V which verifies that the designed filter meets the design goals of attenuation to less than 2.8 V.

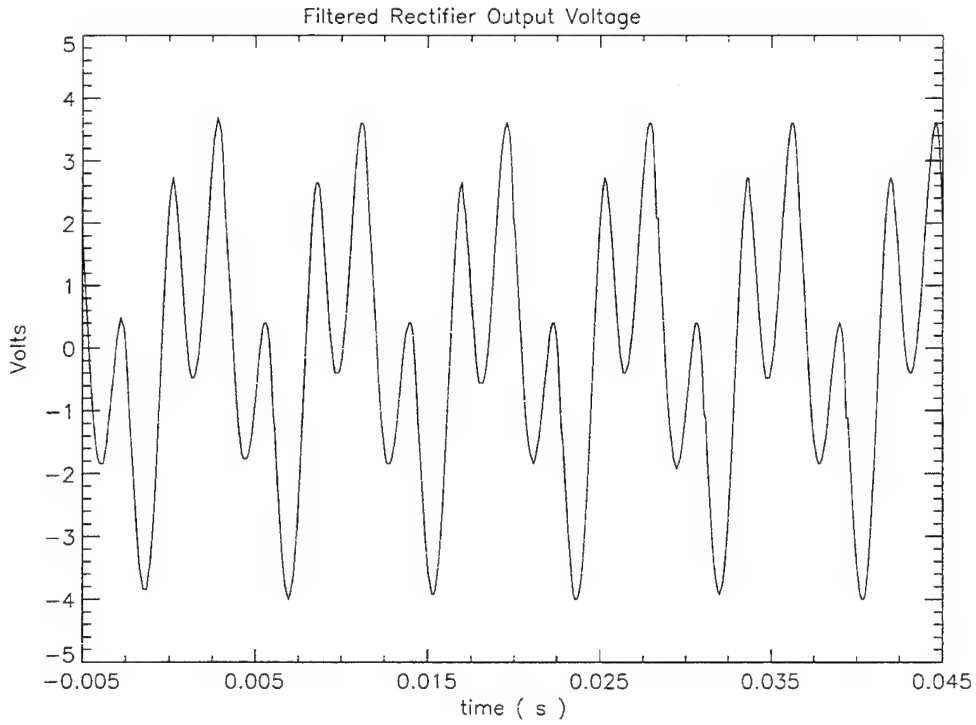


Fig. 40. Filtered rectifier output ripple voltage with 1.6 kW resistive load.

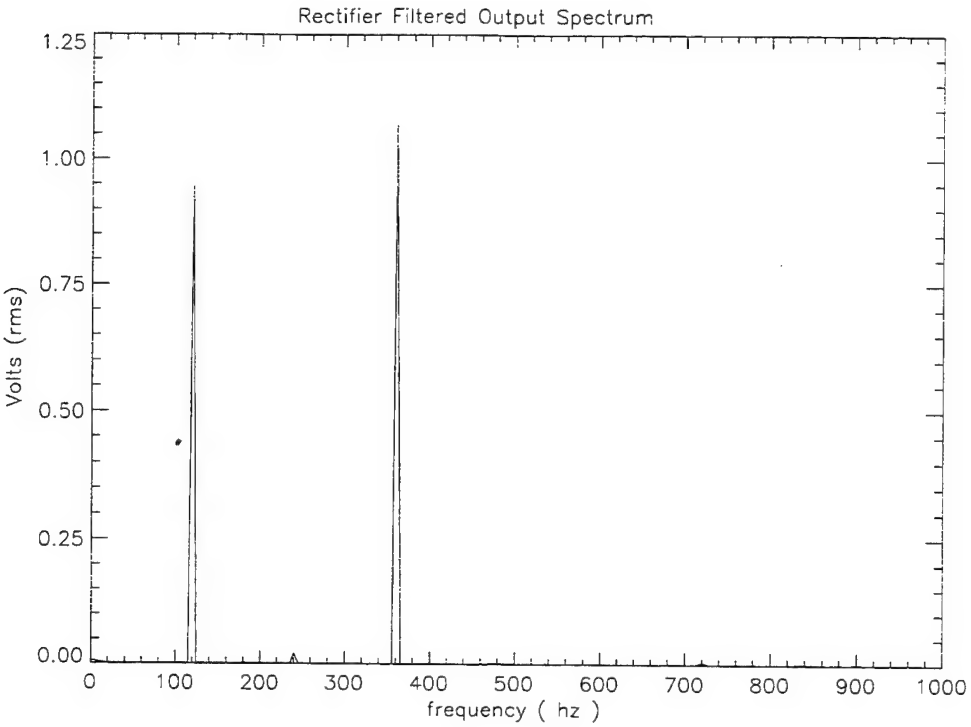


Fig. 41. Filtered rectifier output ripple voltage spectum to 1 khz with 1.6 kW resistive load.

4.2.2. RECTIFIER WITH CONSTANT POWER LOAD

The power measurements obtained from the conventional rectifier circuit loaded with the same 1.6 kW constant power load used for the active pfc circuit are presented in Table 4. The efficiency of the rectifier circuit from utility to load was 99 %. The constant power load resulted in a slightly lower power factor which indicates that the conventional rectifier power factor is susceptible to loads unlike the active pfc circuit analyzed earlier.

Table 4: Conventional rectifier, constant power load, power measurements

Parameter	Value
Utility pf	0.76
Utility power (W)	1582
Output power (W)	1560
Overall Efficiency (%)	99

CHAPTER 5
DISCUSSION AND CONCLUSIONS

The intent of this investigation was to quantify the advantages and disadvantages of three-phase active power factor correction rectification compared to conventional three-phase full-wave bridge rectification for high power applications. A 3 kW active pfc circuit was designed and implemented to demonstrate the issues that are involved with implementing such a design. Some of these issues, specifically the boost switch losses associated with hard-switched power devices, limited the active pfc circuit from supplying more than 1.6 kW of output power. A three-phase bridge rectifier was also fabricated to supply the same load as the active pfc circuit.

The noticeable practical disadvantage with conventional rectifiers is the low power factor they present to the power source. The principal advantage of the rectifier is that it is very efficient (> 97 %) and is capable of drawing tens of kilowatts from its source. The rectifier circuit tested here had a 0.78 pf rating for a resistive load and a 0.76 pf for a constant power load. Passive input filters can be designed to improve the rectifier pf, but the harmonics that the input filter must attenuate are so low in frequency that the required input filter would be physically large. Even then the power factor would not approach the pf provided by an active circuit. Another disadvantage of the rectifier is that its output is not controllable and the voltage will change as a function of load.

The primary advantage of the active pfc circuit is that a very high pf is seen by the utility and the high pf is independent of load. The experimental results confirm that the design presents unity pf with both resistive and constant power loads. Another advantage of the active pfc is that the output voltage is easily regulated by the boost converter portion of the circuit. However these advantages come with penalty. Although the pf is high with the active pfc, the efficiency is low. Compared to the rectifier circuit tested, the active pfc circuit's efficiency is 81 % compared to the conventional rectifier's 97 % for resistive loads. The reduced efficiency is attributed primarily to the boost switch IGBT and snubber losses. The low efficiency limited the active pfc rectifier, utilizing a 100 A, 600 V IGBT as the boost switch, to 1.6 kW. Considering both efficiency and power factor, the active pfc circuit and the conventional rectifier draw similar levels of Volt-Amperes (VA) from their sources to provide power to the identical loads with the active pfc rectifier drawing less. The major difference is that the conventional rectifier draws reactive power and the active pfc rectifier draws real power. These advantages are provided by a more complicated, more expensive, and consequently less reliable design.

In [2], Prasad refers to the stresses imposed on the boost switch as being a "disadvantage of a boost pfc circuit." The results presented here have shown that these stresses render the proposed design practically unfeasible. The losses associated with the boost switch were high and required active cooling in the hard-switched application used here. The limit of a 1.6 kW load for an active three-phase pfc design renders the design unpractical since a single phase source is capable of supplying a 1.6 kW load. For this type of circuit to be feasible, the boost switch requires some type of soft-switch scheme. Different

ways to perform the soft switching exist that need further investigation. One possible solution to the problem is resonant switching, of which a few methods have been proposed. Another possible solution would be to replace the boost diode with a fully controlled switch. If the diode was fully controllable, a control scheme could be designed to ensure that the diode is on before the boost switch turns off to eliminate the destructive transient voltage that the snubber is dissipating. These solutions add more cost and complexity to the design while decreasing reliability.

There are advantages to using active pfc but also disadvantages. Active pfc does have costs that circuits without active pfc do not have, but these costs may be less than penalties imposed by utility companies for loads representing poor power factor and/or high harmonic distortion. Hard-switched active pfc rectifiers are also limited in output power capabilities as compared to conventional diode rectifiers. Many pfc solutions are being investigated, but more effort needs to be placed on implementing these solutions.

REFERENCES

1. N. Mohan, T. M. Undeland, W. P. Robbins, "Power Electronics: Converters, Applications, and Design." John Wiley and Sons; NY, NY, 1989.

2. A. R. Prasad, P. D. Ziogas, S. Manias, " An Active Power Factor Correction Technique for Three-Phase Diode Rectifiers." IEEE Transactions on Power Electronics, Vol. 6, No. 1, Jan 1991, pp. 83 - 92.

3. Analogy®, Inc. "Saber Reference Manual, Release 3.1a." 1987.

4. M. H. Rashid, " Power Electronics: Circuits, Devices, and Applications." Prentice-Hall: Englewood Cliffs, NJ, 1988.

5. Philips Components, " Ferrite Materials and Components Catalog."

6. FUJI, " IGBT Module Application Manual."

APPENDIX A
NODE EQUATIONS FOR SABER SIMULATIONS

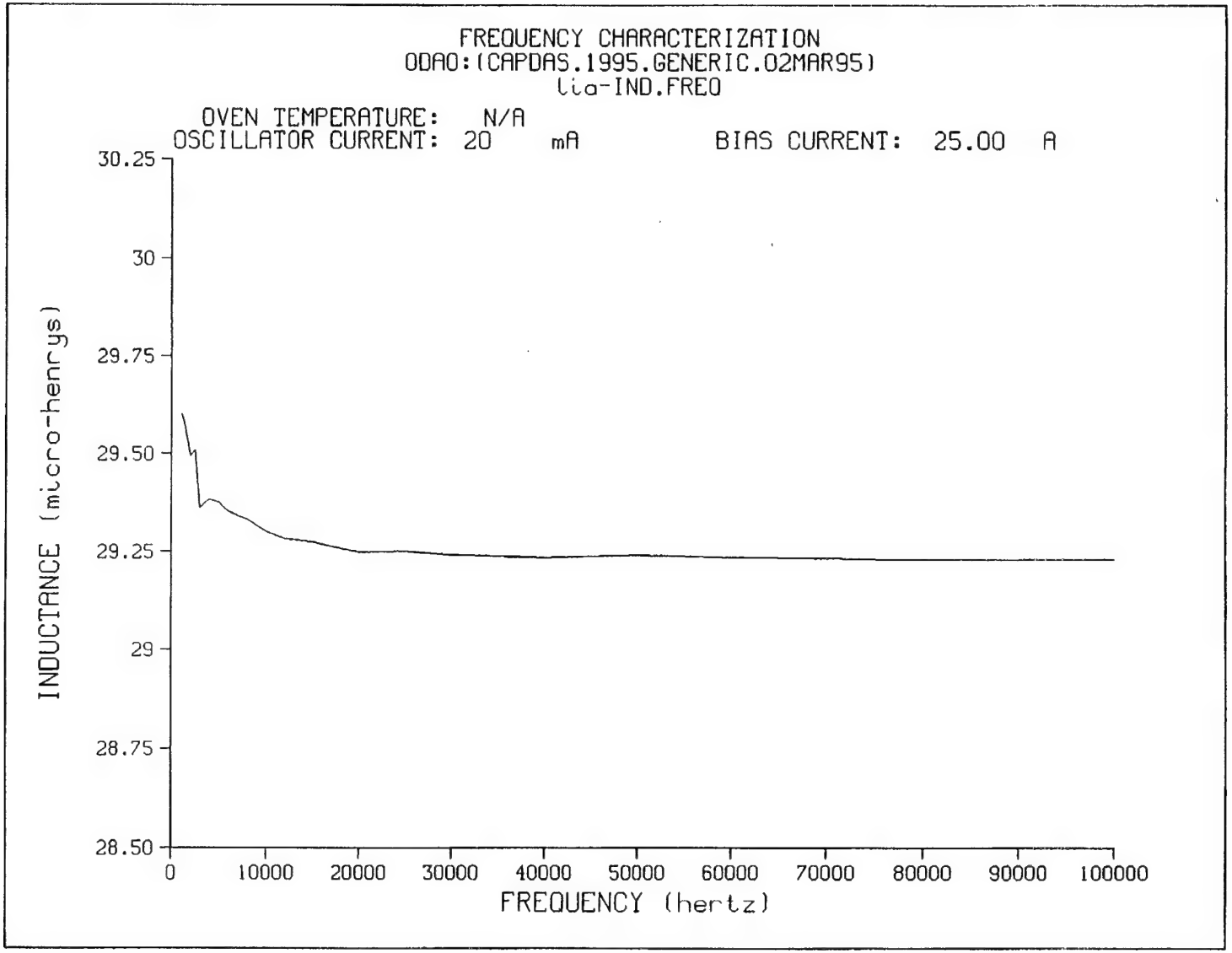
```
#-------------------------------------------------------------------------------
#       BOOST INDUCTOR ANALYSIS CIRCUIT
#-------------------------------------------------------------------------------
#
three_phase.1  phase_a_out phase_b_out phase_c_out neutral =70.7, 60
l.ia     phase_a_out   a_rect_in      = 982u
l.ib     phase_b_out   b_rect_in      = 982u
l.ic     phase_c_out   c_rect_in      = 982u
d.d1     a_rect_in     rect_out
d.d3     b_rect_in     rect_out
d.d5     c_rect_in     rect_out
d.d4     0             a_rect_in
d.d6     0             b_rect_in
d.d2     0             c_rect_in
r.meas rect_out        rect_out_1    =.000001
clock_l4.in            clock:in      = freq=1800,duty=.5,restart=continue
sw_l4.q1               c:in m:0 p:rect_out_1 = roff=1meg, ron=.01,tr=3u,tf=3u
d.db     rect_out_1    dc_out
r.load   dc_out        0             =80
c.dc     dc_out        0             =100u,ic=270
```

```
#-------------------------------------------------------------------------------------------------------
# ACTIVE THREE-PHASE POWER FACTOR CORRECTION CIRCUIT
#-------------------------------------------------------------------------------------------------------
#
three_phase.1  phase_a_out phase_b_out phase_c_out neutral =70.7, 60
l.fa     phase_a_out   filter_a_out    =66u
l.fb     phase_b_out   filter_b_out    =66u
l.fc     phase_c_out   filter_c_out    =66u
c.fa     filter_a_out  neutral         =11u
c.fb     filter_b_out  neutral         =11u
c.fc     filter_c_out  neutral         =11u
r.dc1    filter_a_out  0               =10meg
r.dc2    filter_b_out  0               =10meg
r.dc3    filter_c_out  0               =10meg
l.ia     filter_a_out  a_rect_in       = 32u
l.ib     filter_b_out  b_rect_in       = 32u
l.ic     filter_c_out  c_rect_in       = 32u
pwld.d1                a_rect_in       rect_out
pwld.d3                b_rect_in       rect_out
pwld.d5                c_rect_in       rect_out
pwld.d4                0               a_rect_in
pwld.d6                0               b_rect_in
pwld.d2                0               c_rect_in
r.meas rect_out        rect_out_1      =.000001
clock_l4.in            clock:in        = freq=24000,duty=.5,restart=continue
sw_l4.q1               c:in m:0 p:rect_out_1 = roff=1meg, ron=.01,tr=2u,tf=3u
pwld.db                rect_out_1      dc_out
r.load   dc_out        0               =29
c.dc     dc_out        0               =866u,ic=270
```

```
#-------------------------------------------------------------------------------
#  3 PHASE RECTIFIER WITHOUT FILTERING
#-------------------------------------------------------------------------------
#
three_phase.1  phase_a_in phase_b_in phase_c_in neutral =169.7, 60
pwld.d1              phase_a_in    rect_out
pwld.d3              phase_b_in    rect_out
pwld.d5              phase_c_in    rect_out
pwld.d4              0             phase_a_in
pwld.d6              0             phase_b_in
pwld.d2              0             phase_c_in
r.load  dc_out       load_l                    =26
l.load  load_l       0                         =.1u
```

```
#-------------------------------------------------------------------------------
#  3 PHASE RECTIFIER WITH OUTPUT FILTER
#-------------------------------------------------------------------------------
#
three_phase.1  phase_a_in phase_b_in phase_c_in neutral =169.7, 60
pwld.d1              phase_a_in    rect_out
pwld.d3              phase_b_in    rect_out
pwld.d5              phase_c_in    rect_out
pwld.d4              0             phase_a_in
pwld.d6              0             phase_b_in
pwld.d2              0             phase_c_in
l.le    rect_out     dc_out                    =1.03m
c.ce    dc_out       0                         =1250u
r.load  dc_out       load_l                    =26
l.load  load_l       0                         =.1u
```

APPENDIX B
INDUCTOR ELECTICAL CHARACTERIZATION CURVES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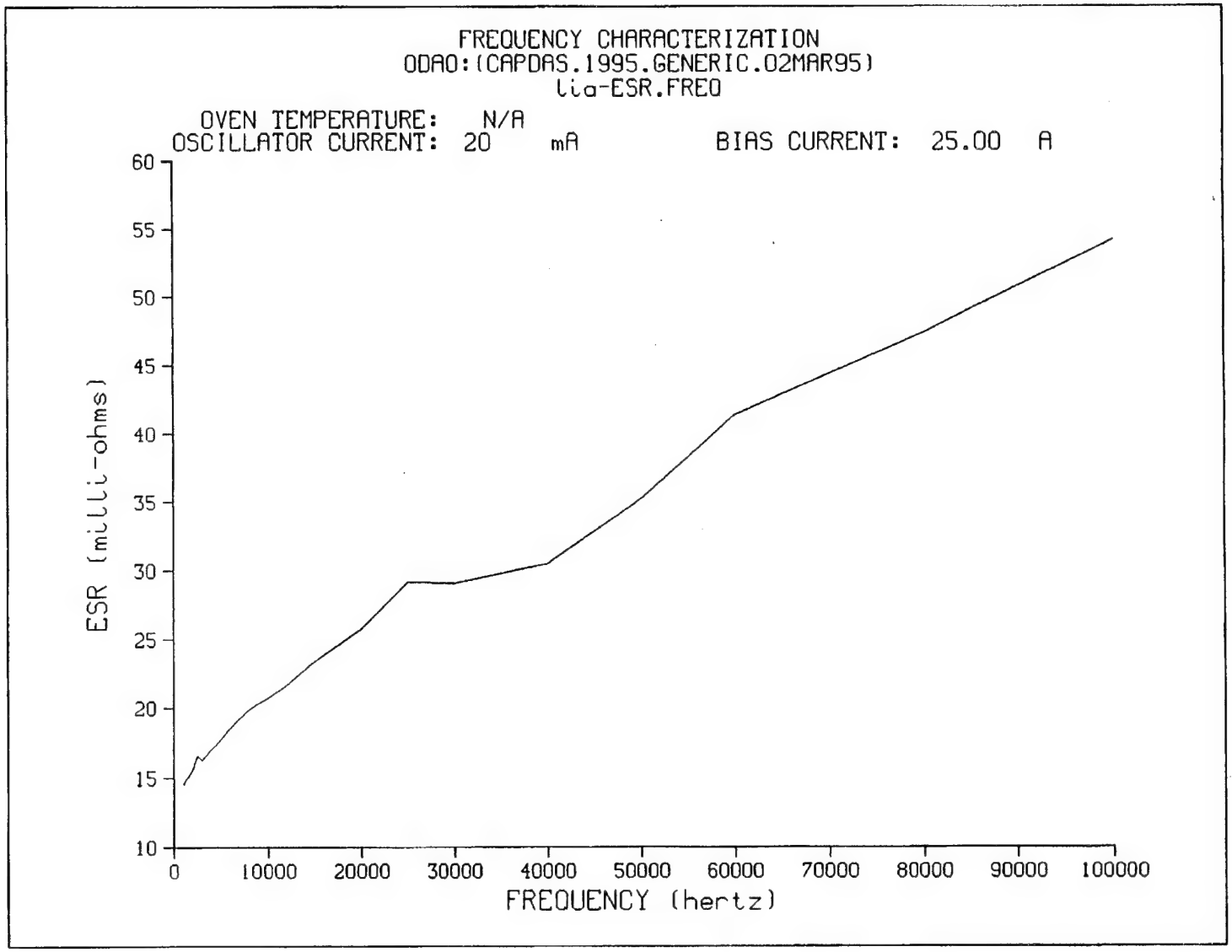
OVEN TEMPERATURE: N/A
OSCILLATOR CURRENT: 20 mA
BIAS CURRENT: 25.00 A
INDUCTANCE (micro-henrys)
30.25
30
29.75
29.50
29.25
29
28.75
28.50
0
10000
20000
30000
40000
50000
60000
70000
80000
90000
100000
FREQUENCY (hertz)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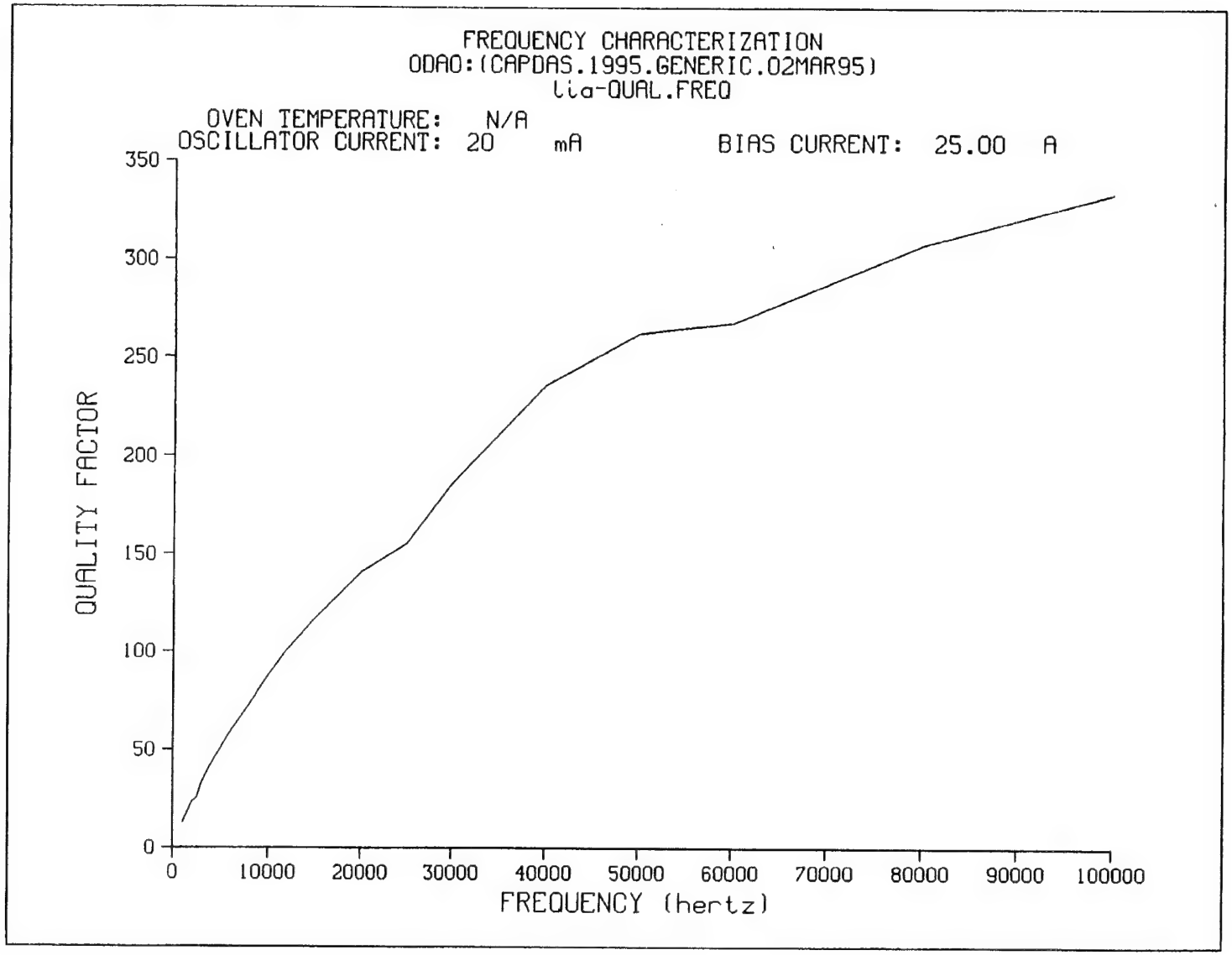
lia-ESR.FREQ
OVEN TEMPERATURE: N/A
OSCILLATOR CURRENT: 20 mA
BIAS CURRENT: 25.00 A
ESR (milli-ohms)
60
55
50
45
40
35
30
25
20
15
10
0
10000
20000
30000
40000
50000
60000
70000
80000
90000
100000
FREQUENCY (hertz)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lia-QUAL.FREQ
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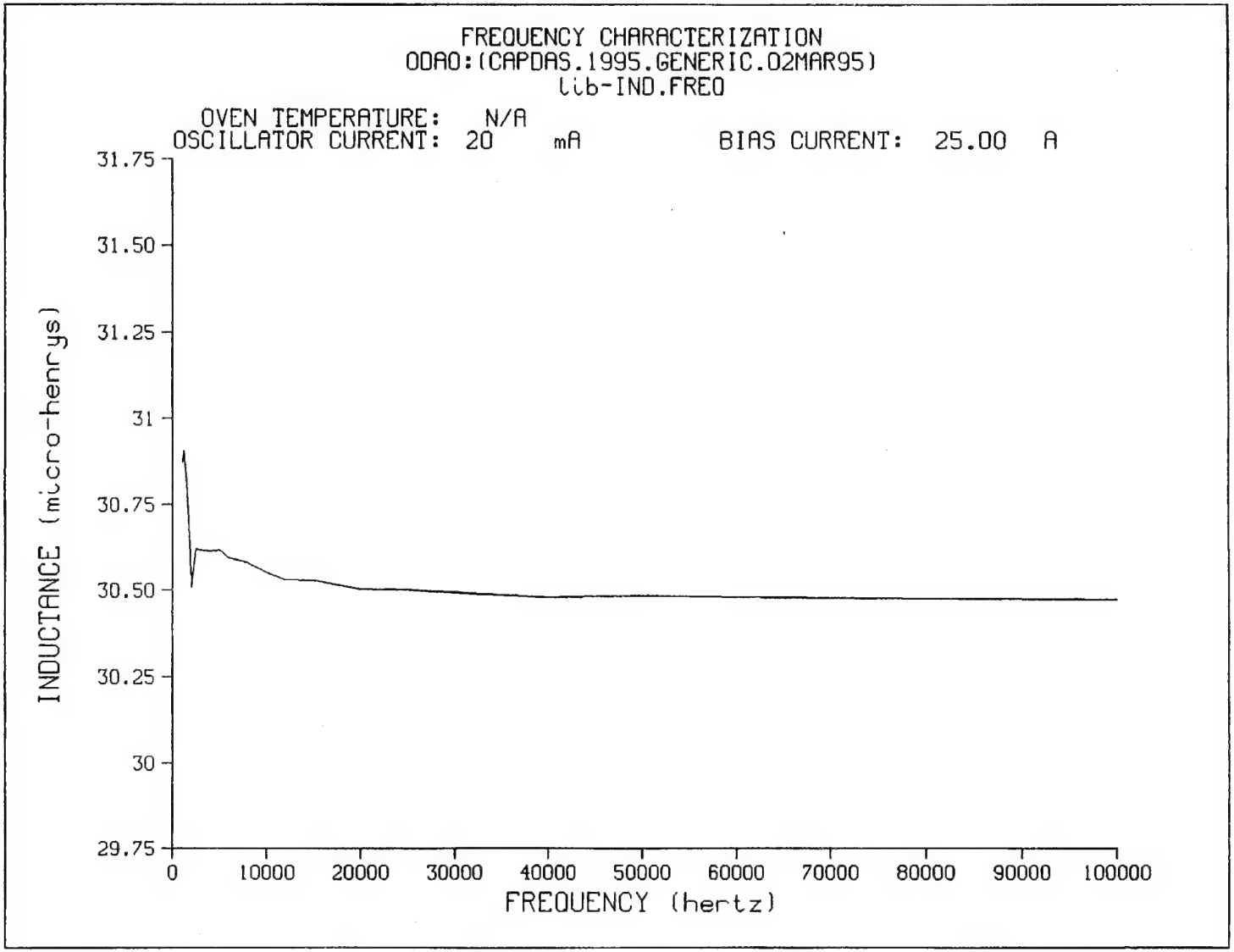
OSCILLATOR CURRENT: 20 mA
BIAS CURRENT: 25.00 A
QUALITY FACTOR
350
300
250
200
150
100
50
0
0
10000
20000
30000
40000
50000
60000
70000
80000
90000
100000
FREQUENCY (hertz)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BIAS CURRENT: 25.00 A
INDUCTANCE (micro-henrys)
31.75
31.50
31.25
31
30.75
30.50
30.25
30
29.75
0
10000
20000
30000
40000
50000
60000
70000
80000
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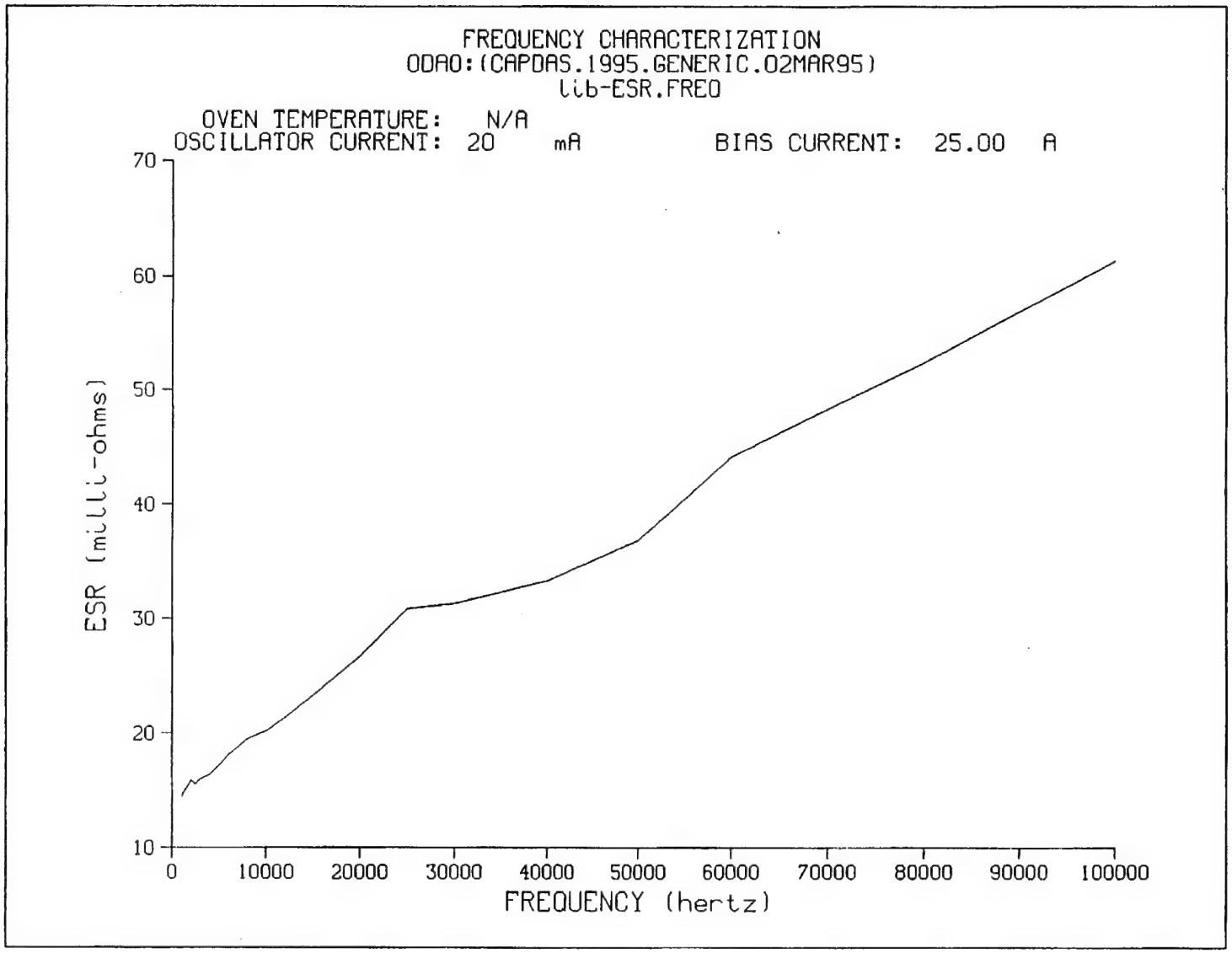
100000
FREQUENCY (hertz)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BIAS CURRENT: 25.00 A
ESR (milli-ohms)
70
60
50
40
30
20
10
0
10000
20000
30000
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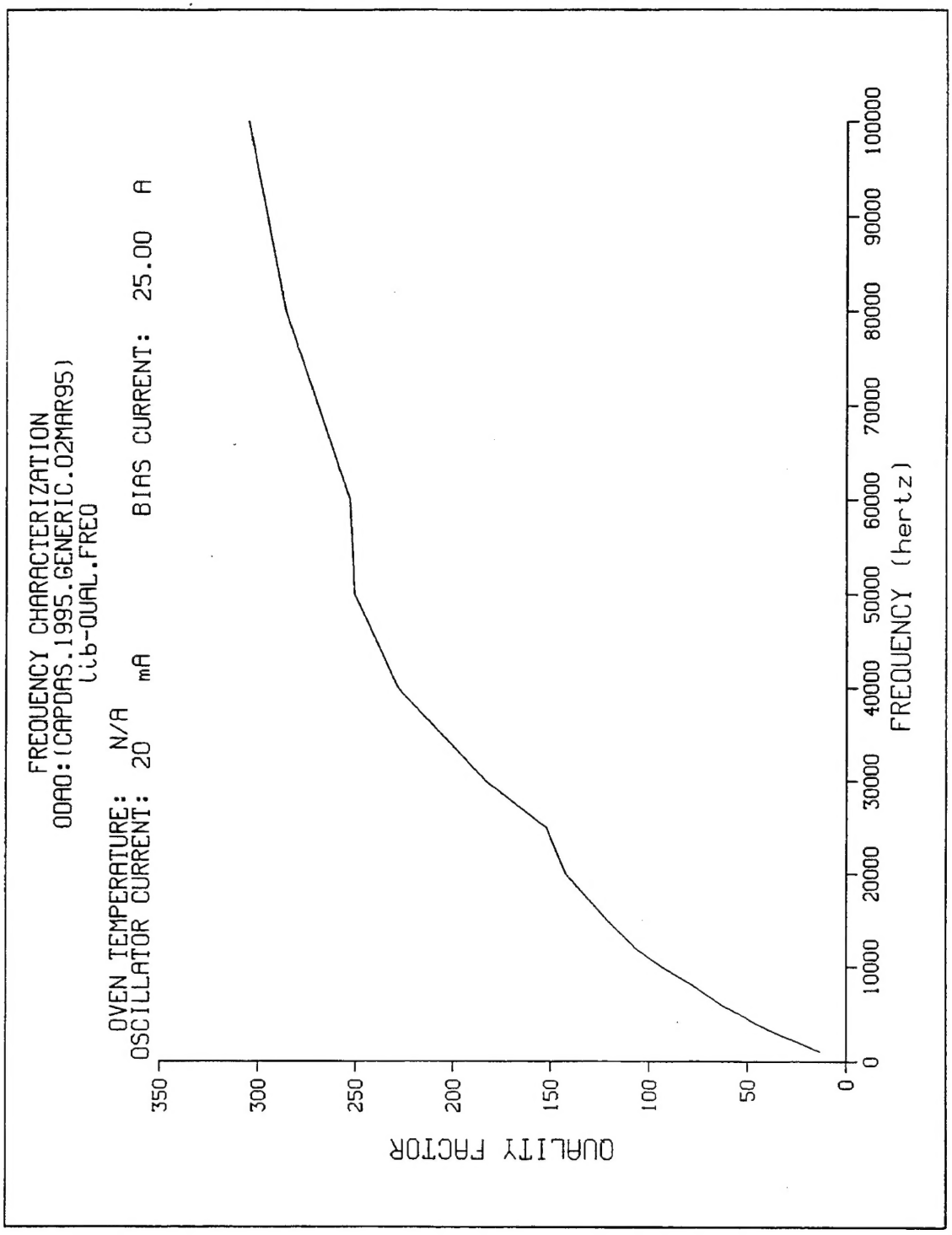
50000
60000
70000
80000
90000
100000
FREQUENCY (hertz)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BIAS CURRENT: 25.00 A
QUALITY FACTOR
350
300
250
200
150
100
50
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20000
30000
40000
50000
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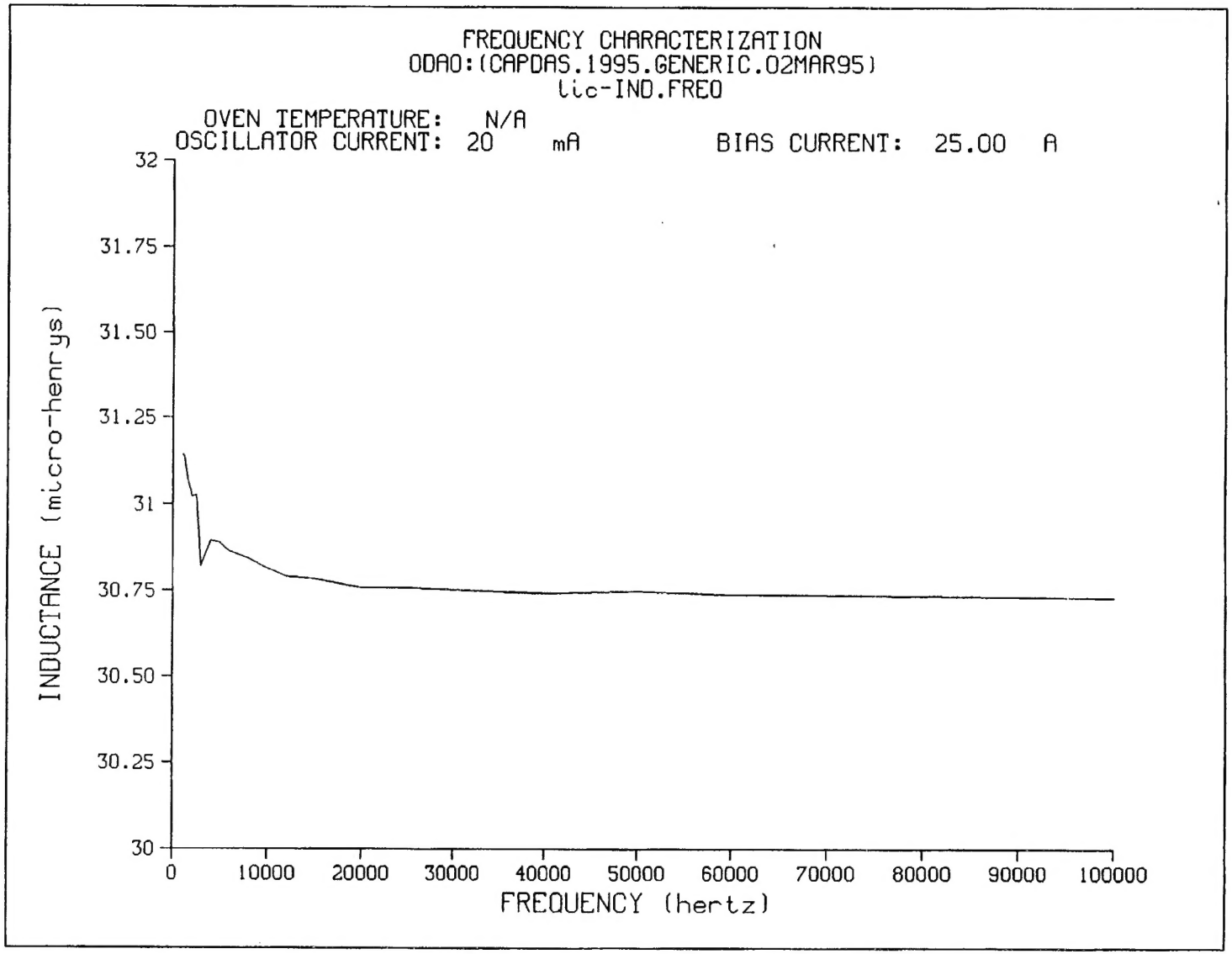
70000
80000
90000
100000
FREQUENCY (hertz)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tic-IND.FREQ
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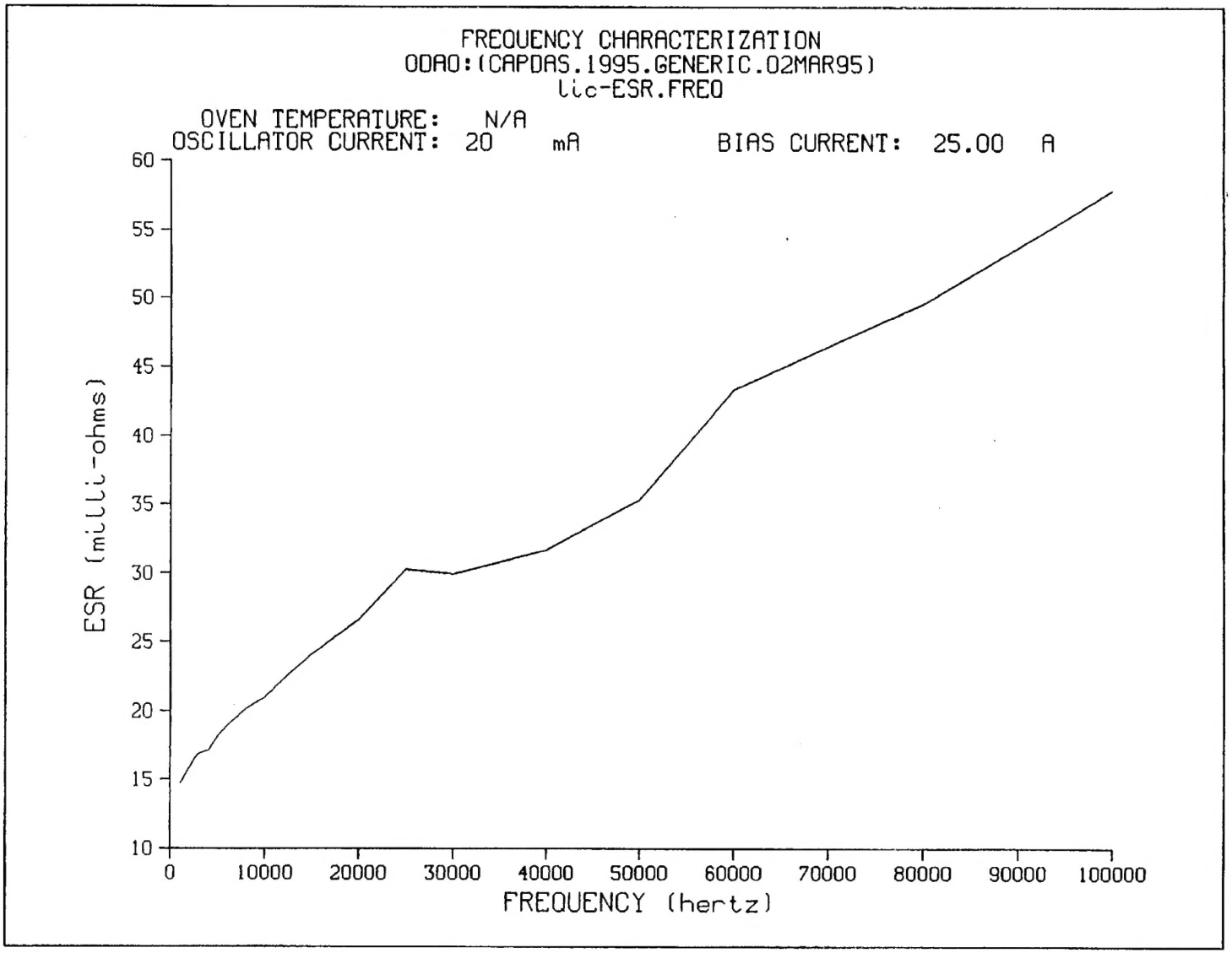
BIAS CURRENT: 25.00 A
INDUCTANCE (micro-henrys)
32
31.75
31.50
31.25
31
30.75
30.50
30.25
30
0
10000
20000
30000
40000
50000
60000
70000
80000
90000
100000
FREQUENCY (hertz)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OSCILLATOR CURRENT: 20 mA
BIAS CURRENT: 25.00 A
ESR (milli-ohms)
60
55
50
45
40
35
30
25
20
15
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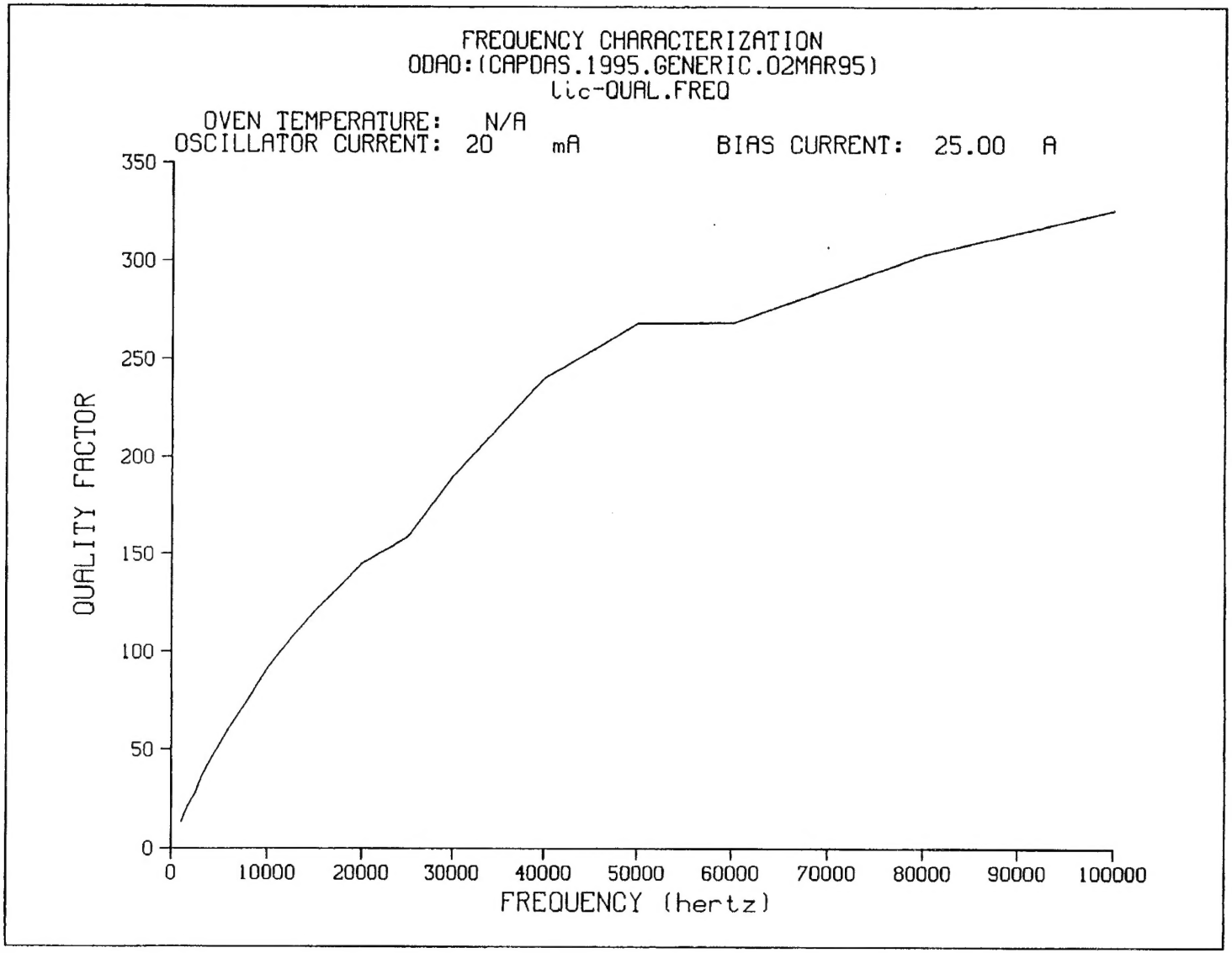
FREQUENCY (hertz)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QUALITY FACTOR
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300
250
200
150
100
50
0
0
10000
20000
30000
40000
50000
60000
70000
80000
90000
100000
FREQUENCY (hertz)